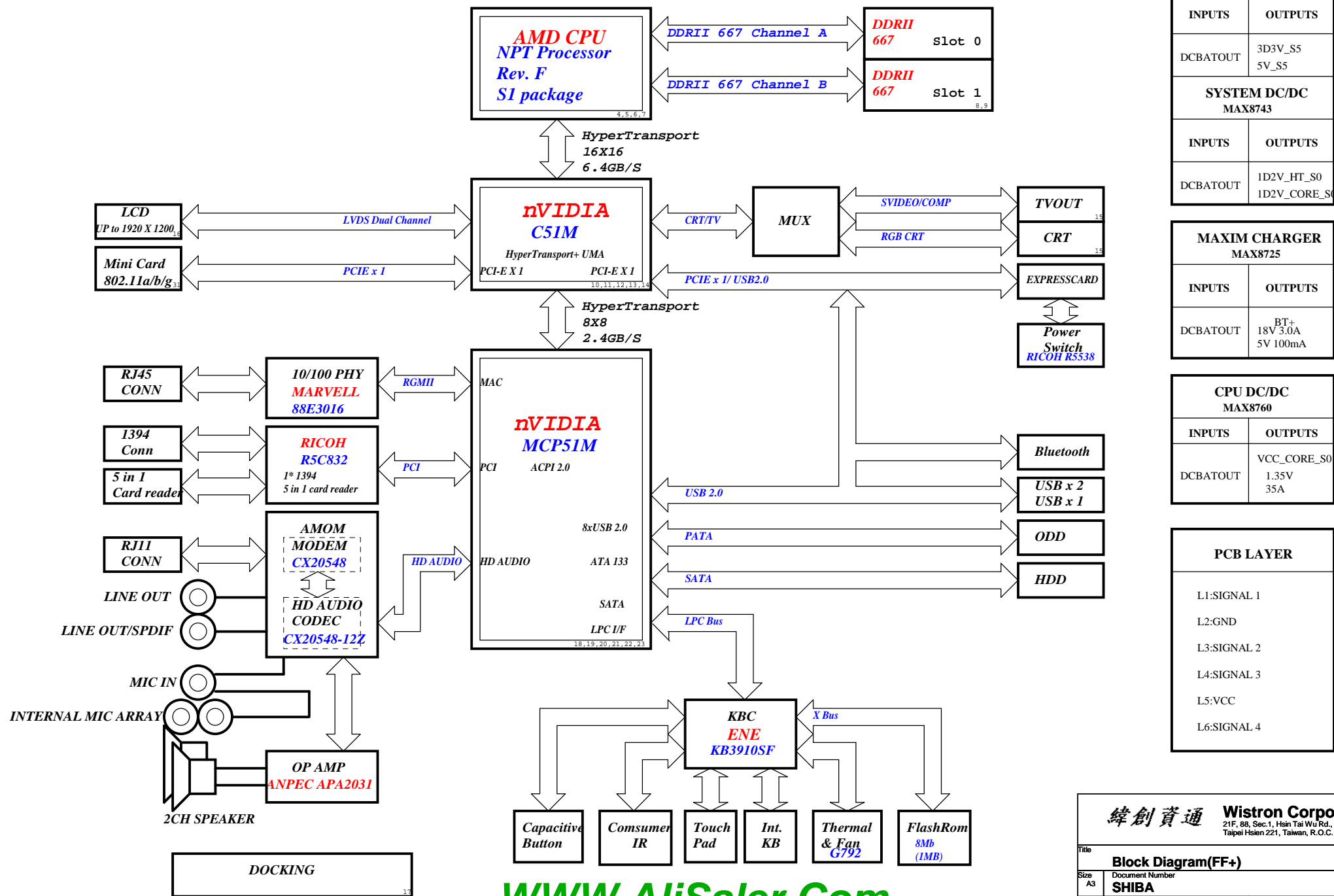


Shiba Block Diagram(DF)



D

D

C

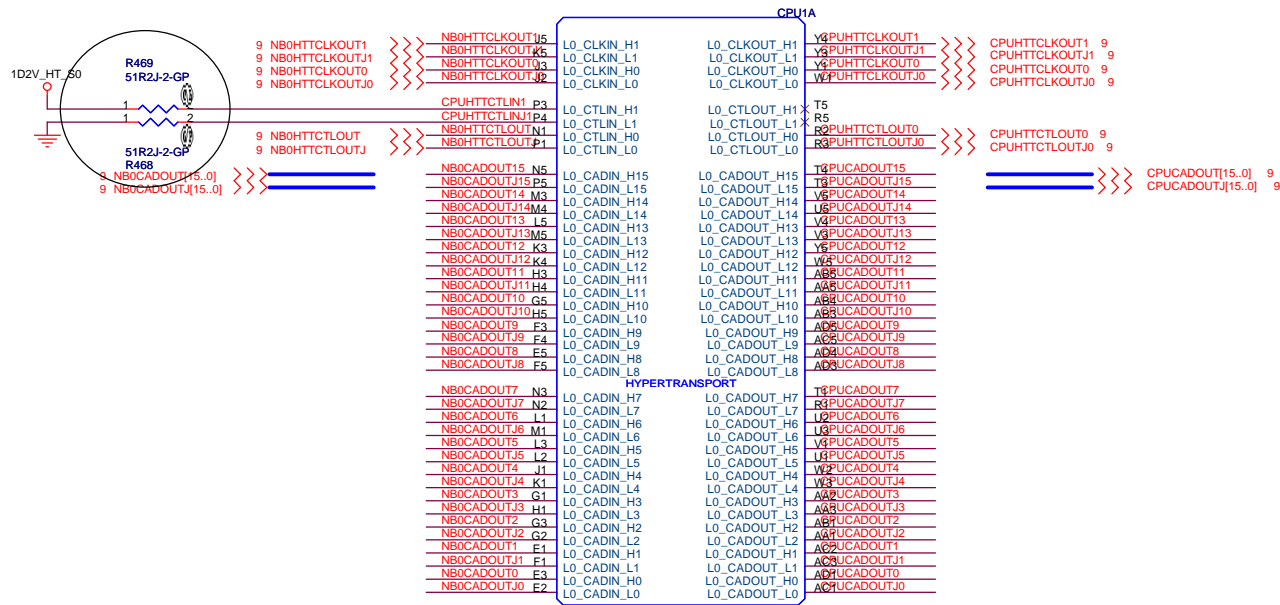
C

B

B

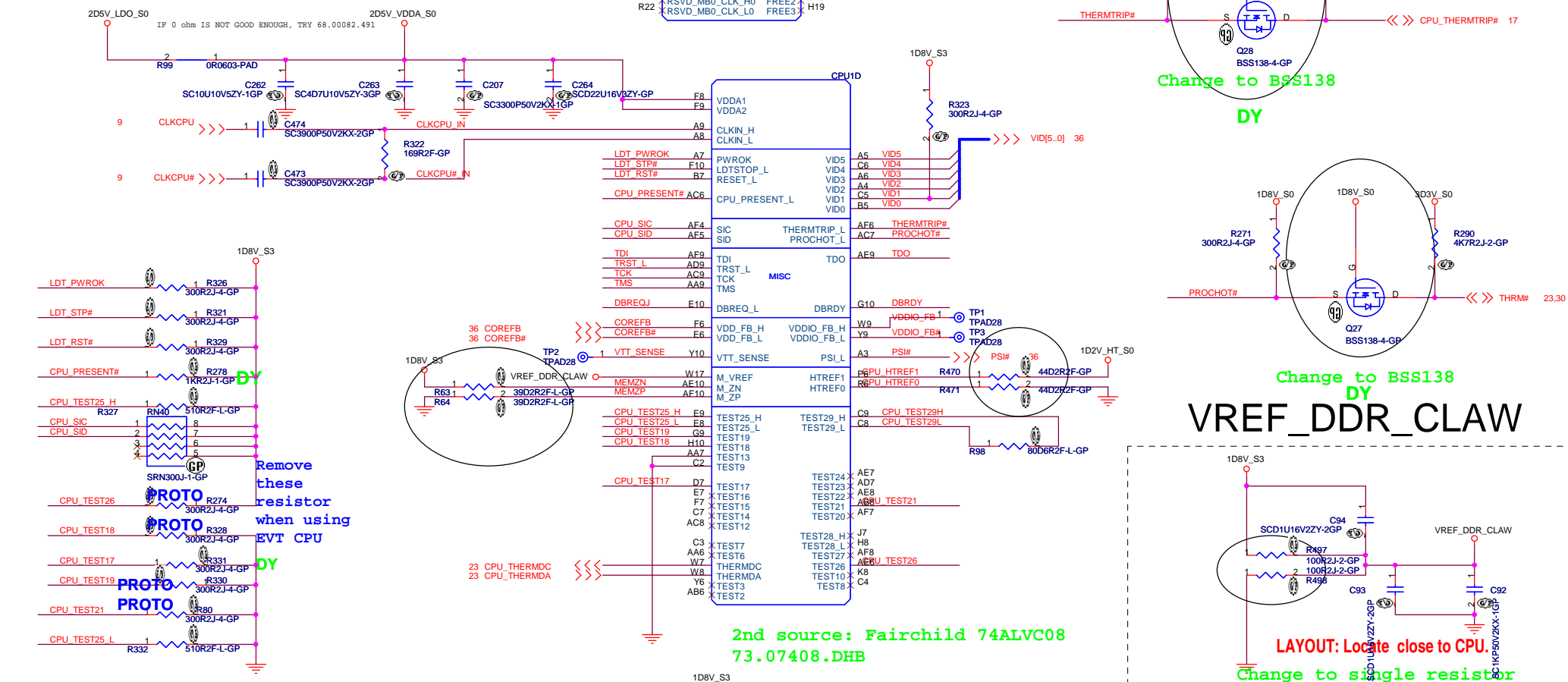
A

A

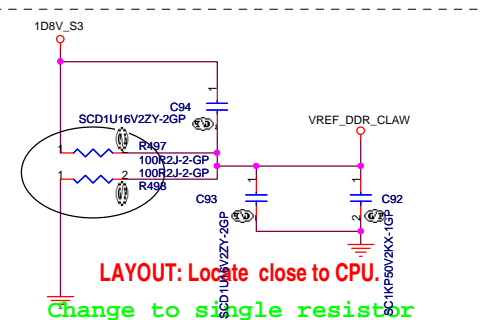
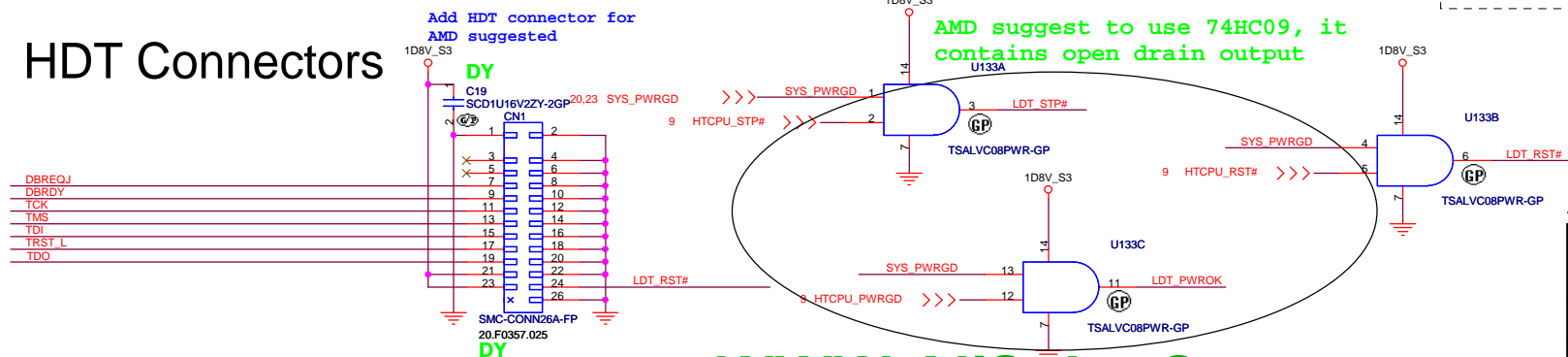


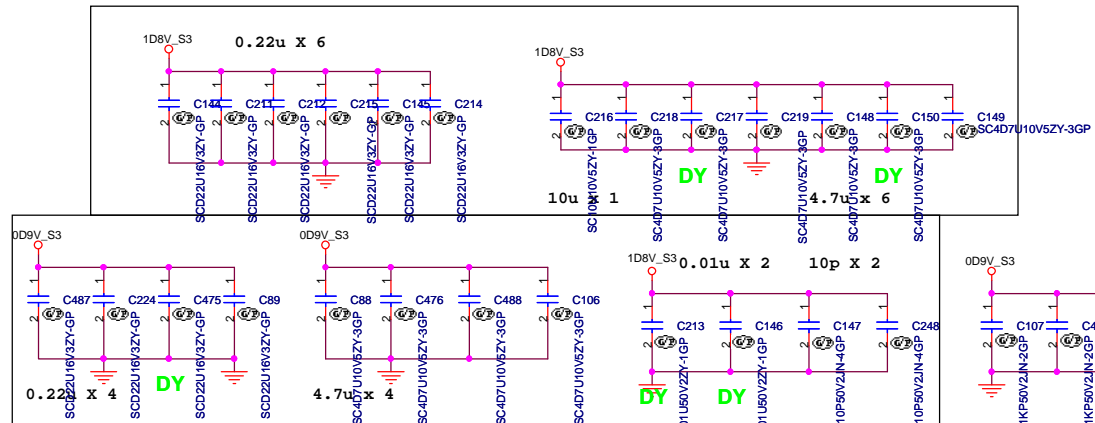
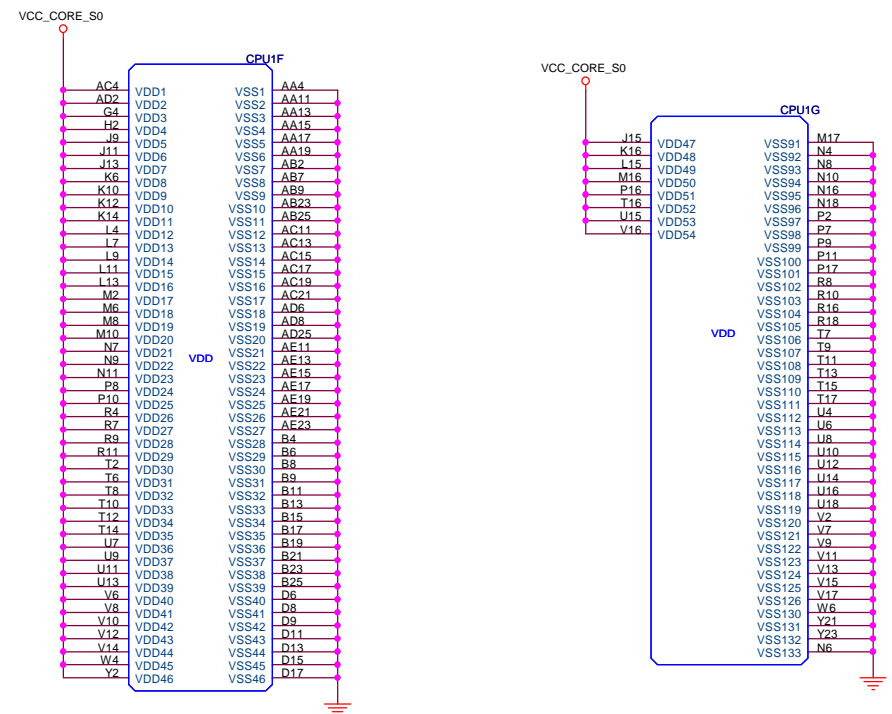
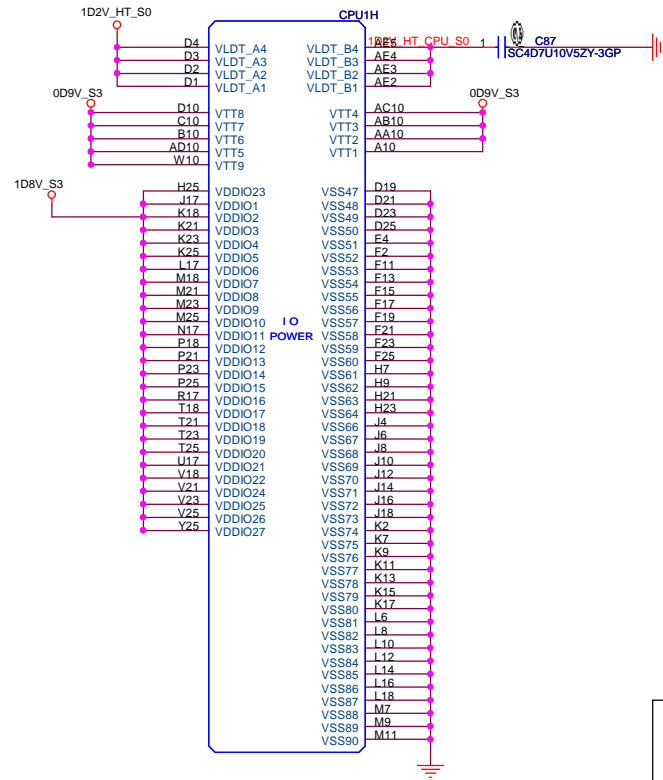


Title			
CPU(2/4) DDR II			
Size A3	Document Number SHIBA		Rev SC
Date:	Friday, February 24, 2006	Sheet 4 of	44

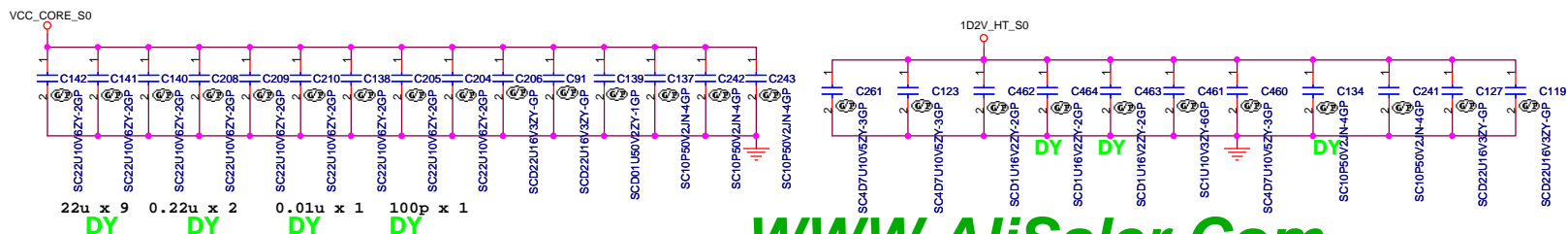


HDT Connectors



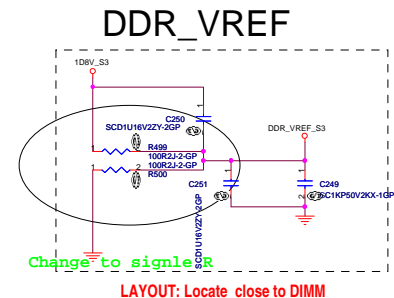
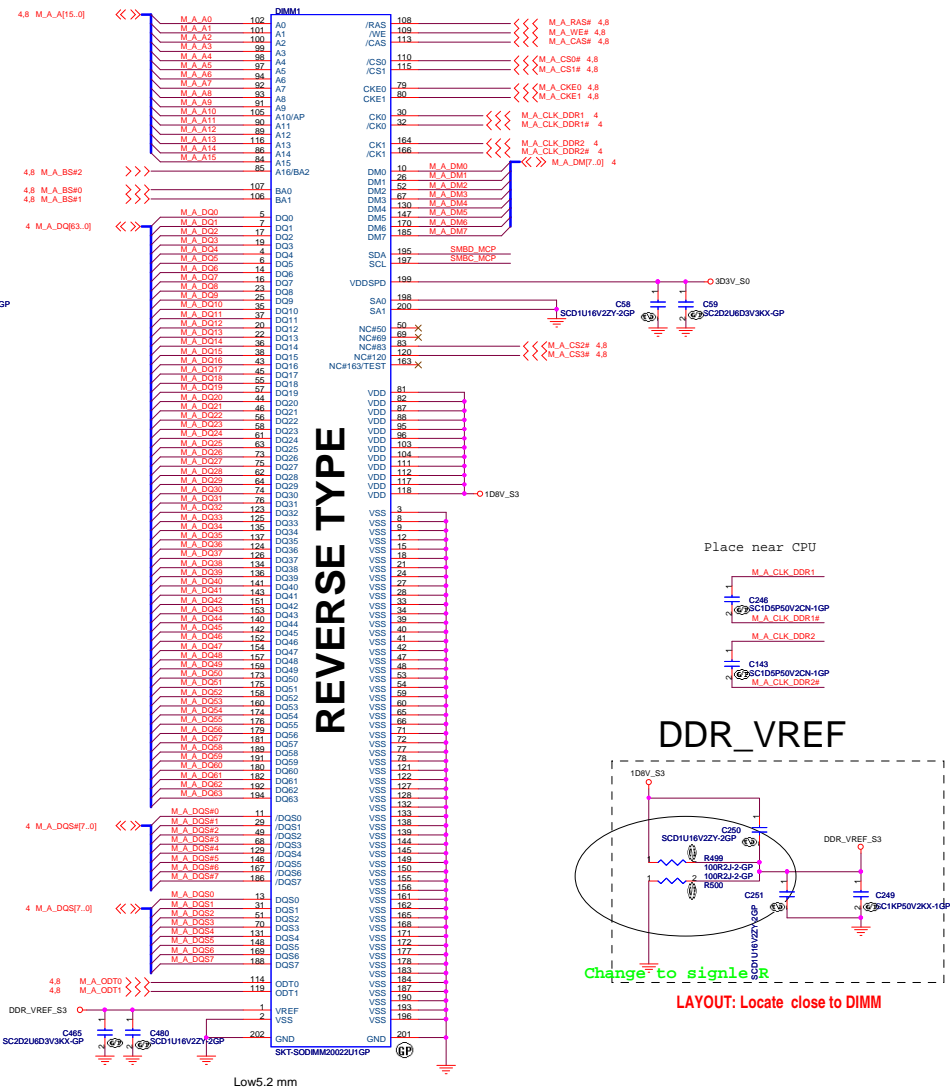


LAYOUT: Place on backside of processor.



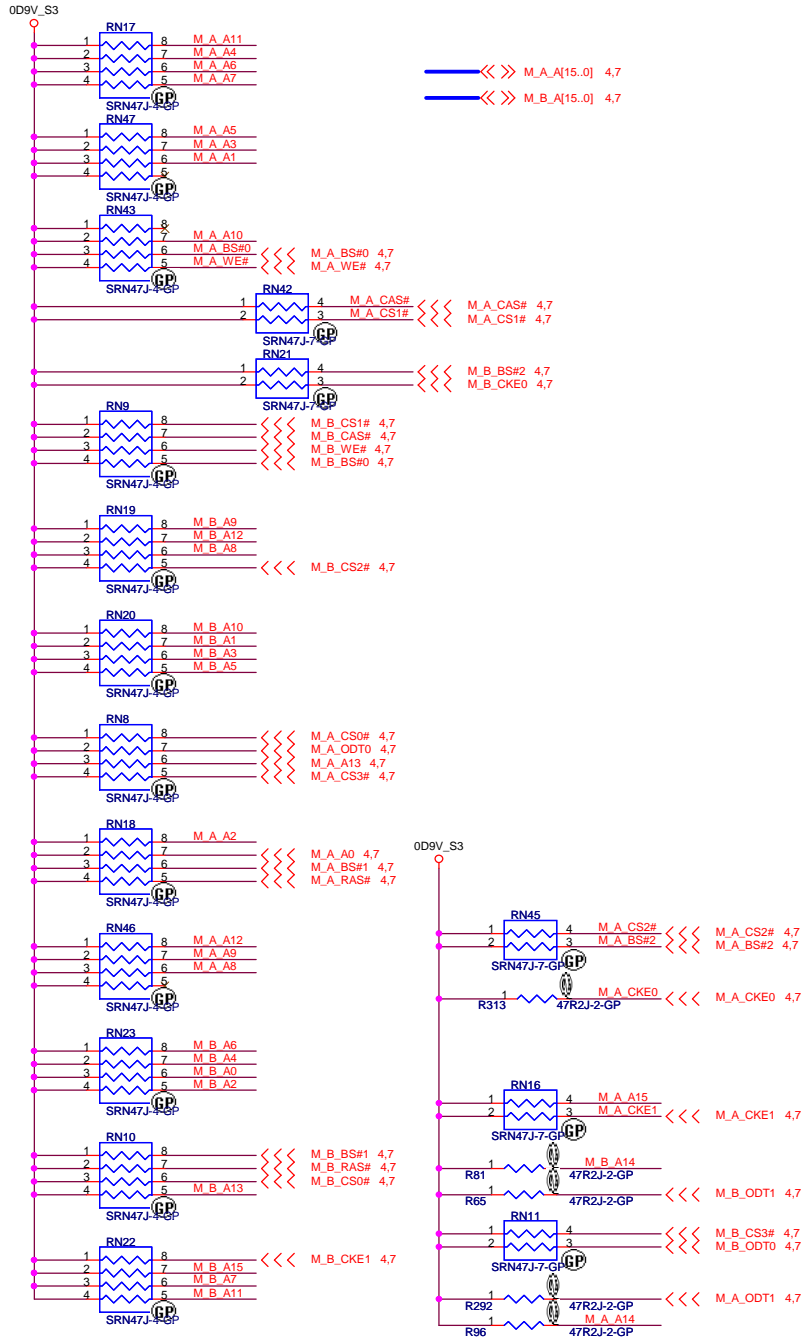
<Variant Name>

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 231, Taiwan, R.O.C.	
Title	CPU(4/4) POWER
Size	Document Number
A3	SHIBA
Date: Friday, February 24, 2006	Sheet 6 of 44



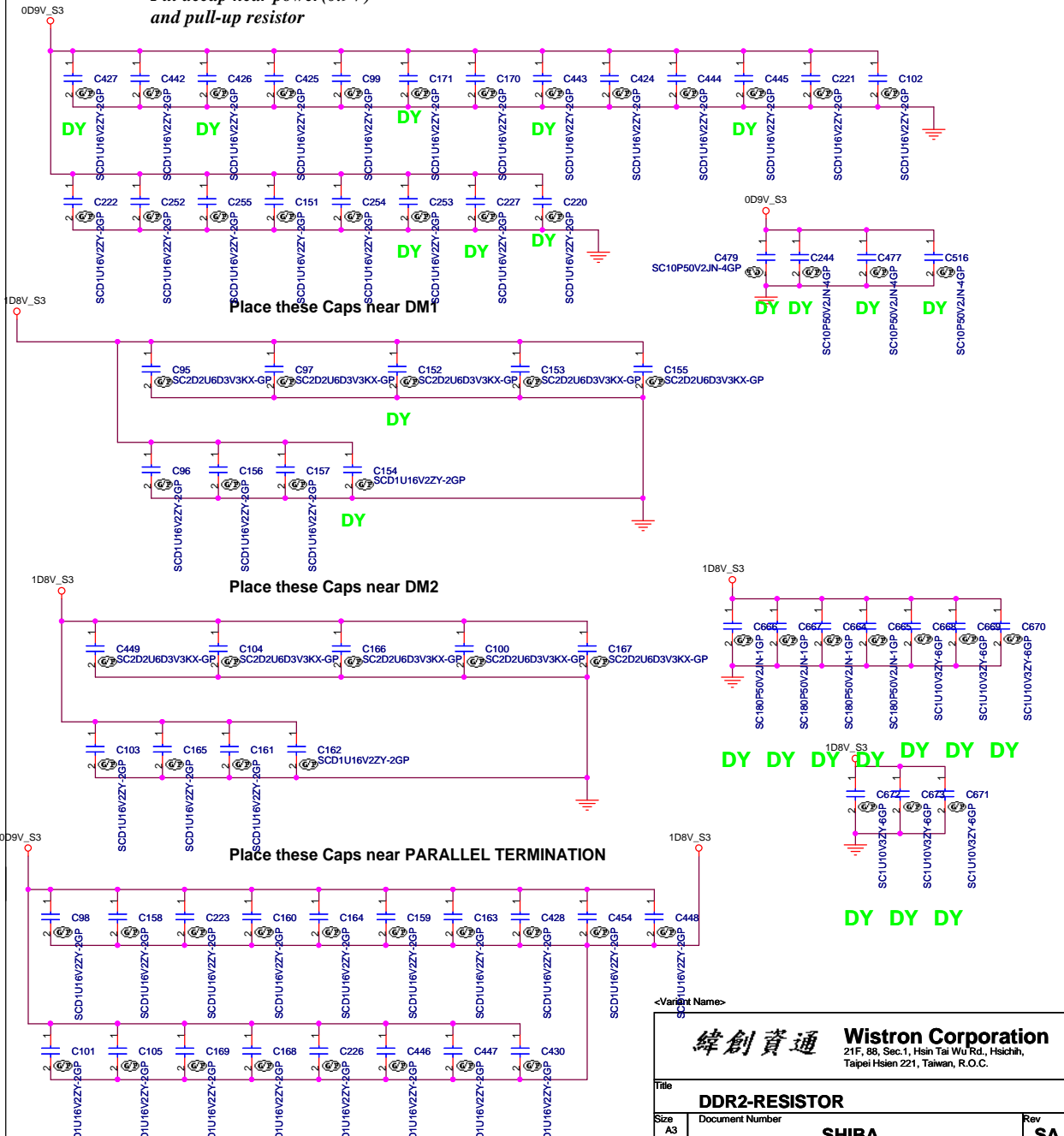
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

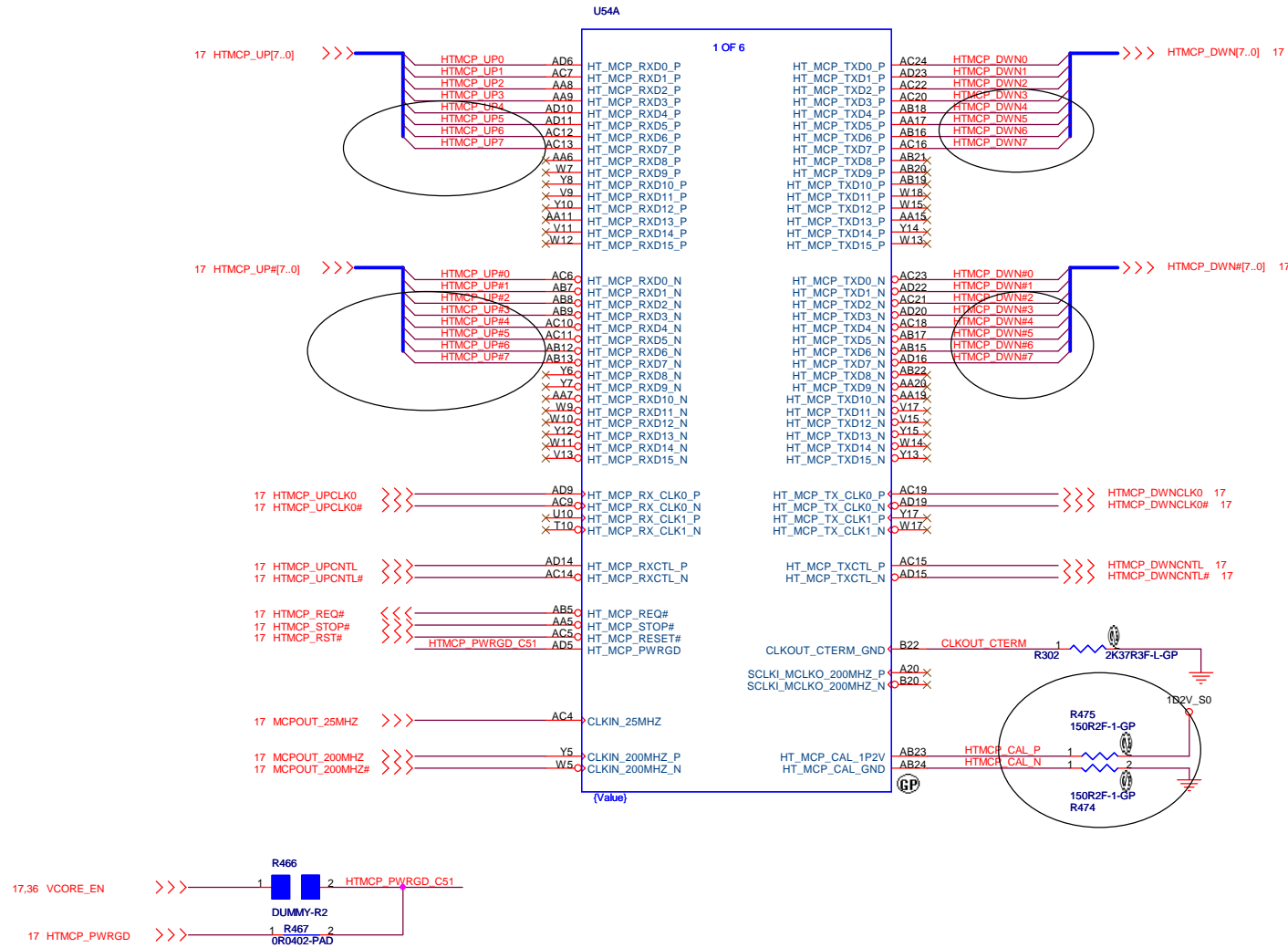
Put decap near power(0.9V) and pull-up resistor

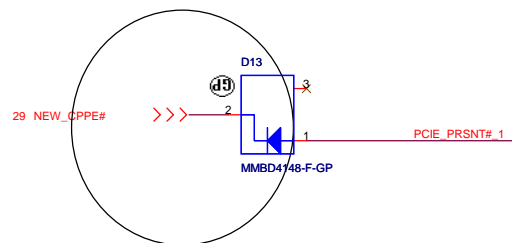


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
DDR2-RESISTOR	
Title Size A3	Document Number SHIBA
Date: Friday, February 24, 2006	Rev SA
Sheet 8 of 44	

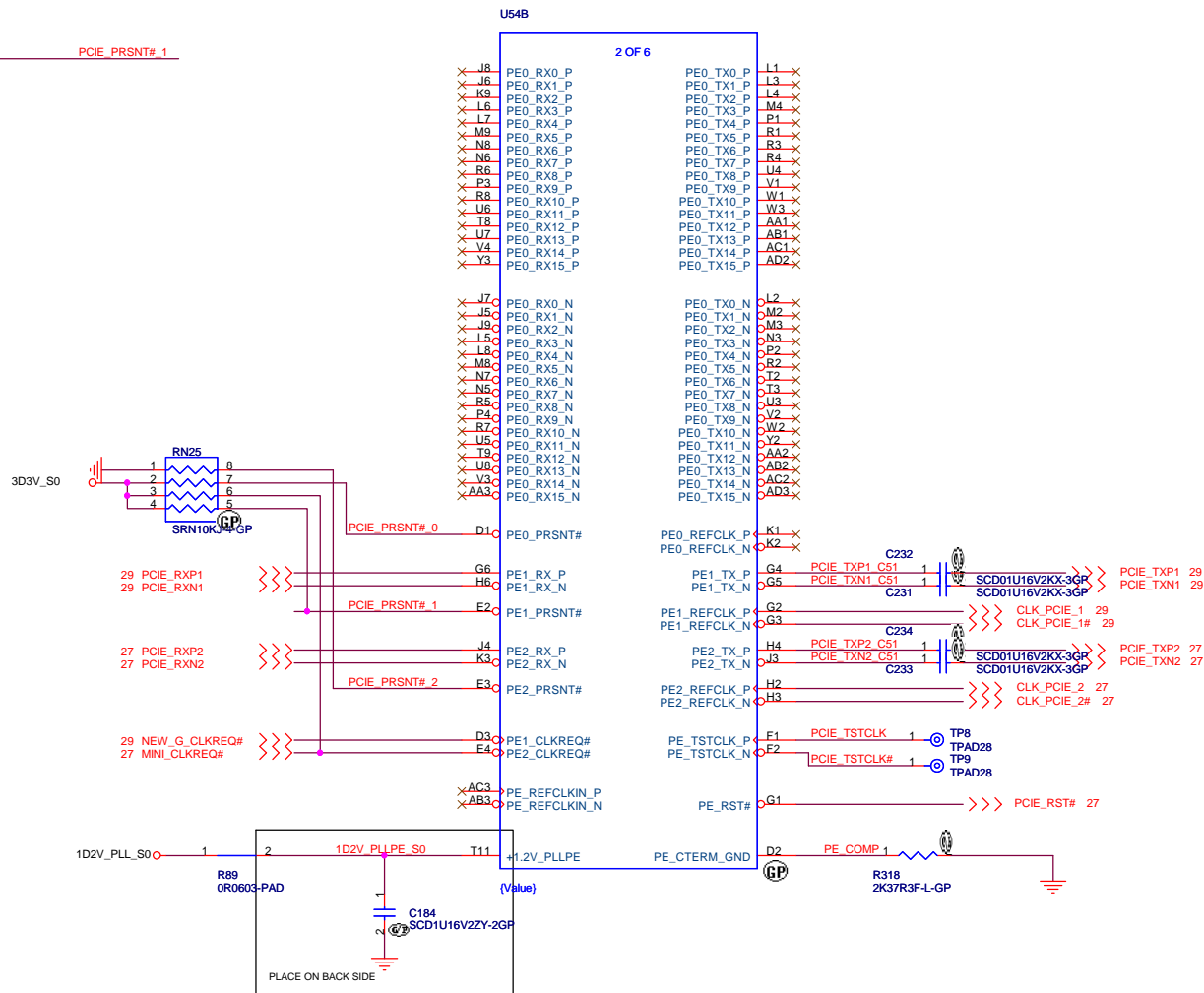


Title		
C51M(1/5) HT CPU		
Size A3	Document Number SHIBA	Rev SC
Date: Friday, February 24, 2006	Sheet 9	of 44



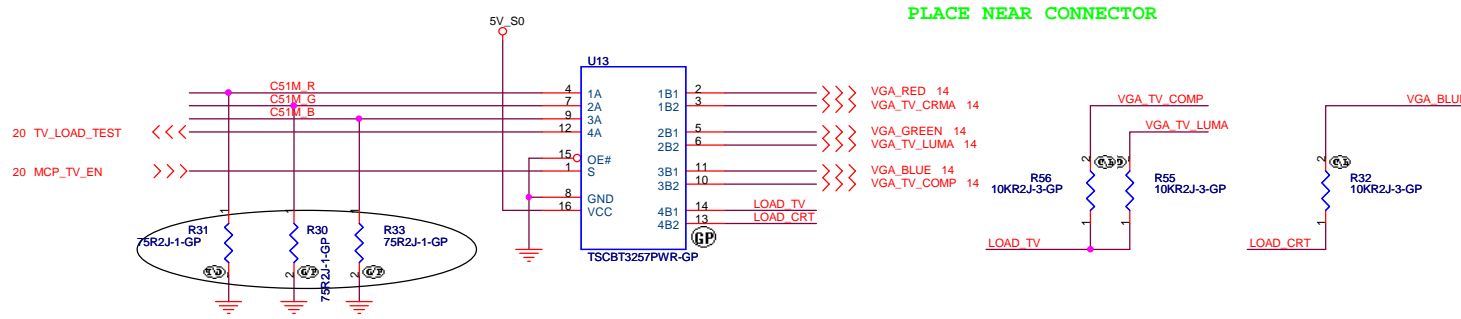
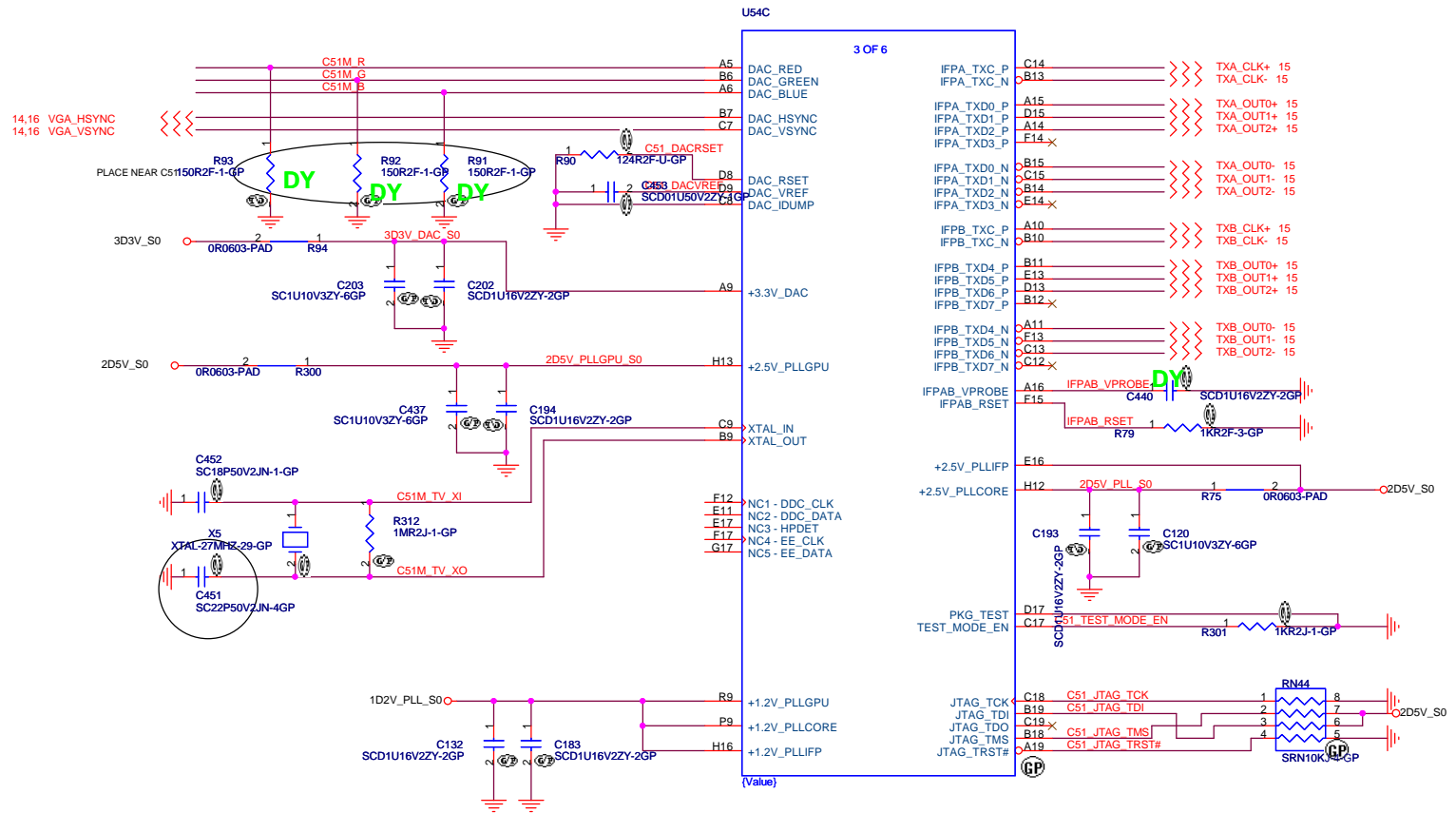


CHECK LEAKAGE CURRENT



<Variant Name>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: C51M(3/5)PCIE			
Size: A3	Document Number: SHIBA		Rev: SA
Date: Monday, February 27, 2006	Sheet: 11	of: 44	



<Variant Name>


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **C51M(4/5)CRT/LVDS**

Size: A3
Document Number: **SHIBA**
Date: Wednesday, March 15, 2006

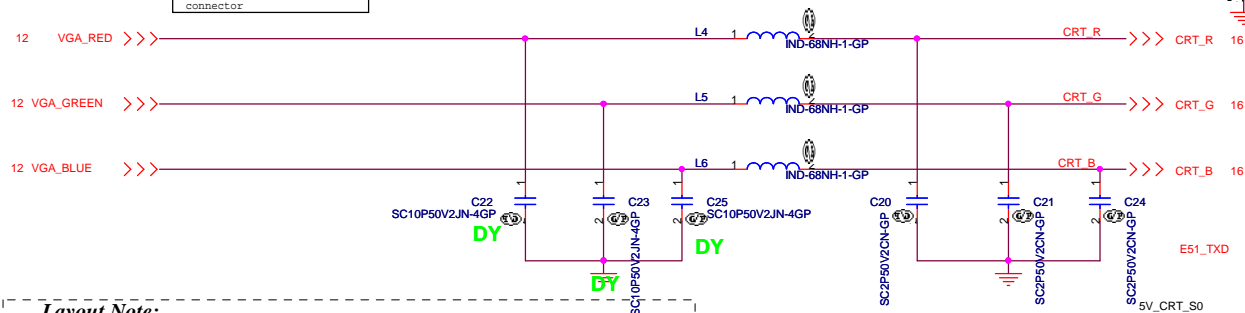
Rev: SA
Sheet: 12 of 44



		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
C51M(5/5)POWER			
Size	Document Number	Rev	
A3	SHIBA	SA	
Date:	Saturday, February 18, 2006	Sheet	13 of 44

CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

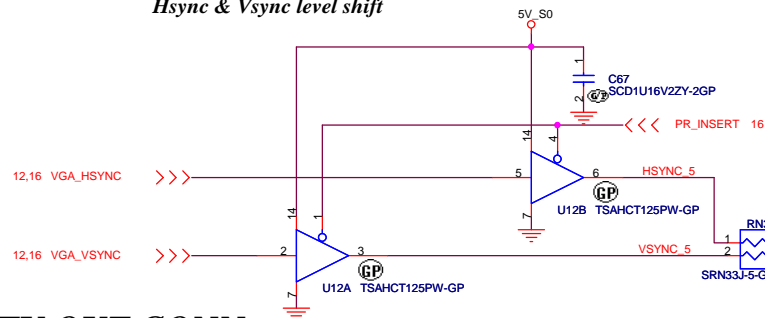


Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.

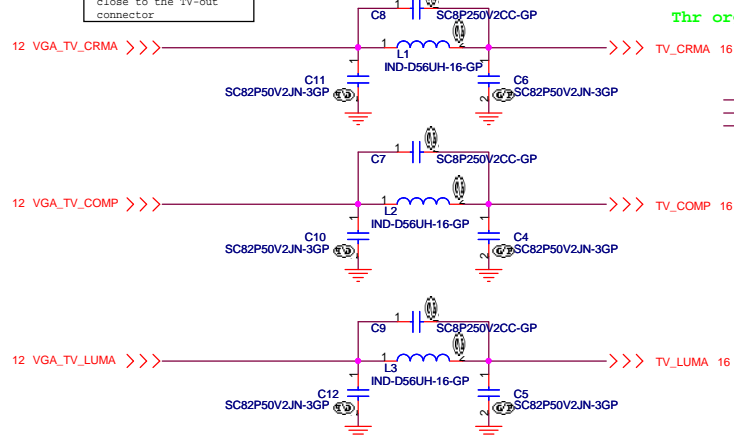
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

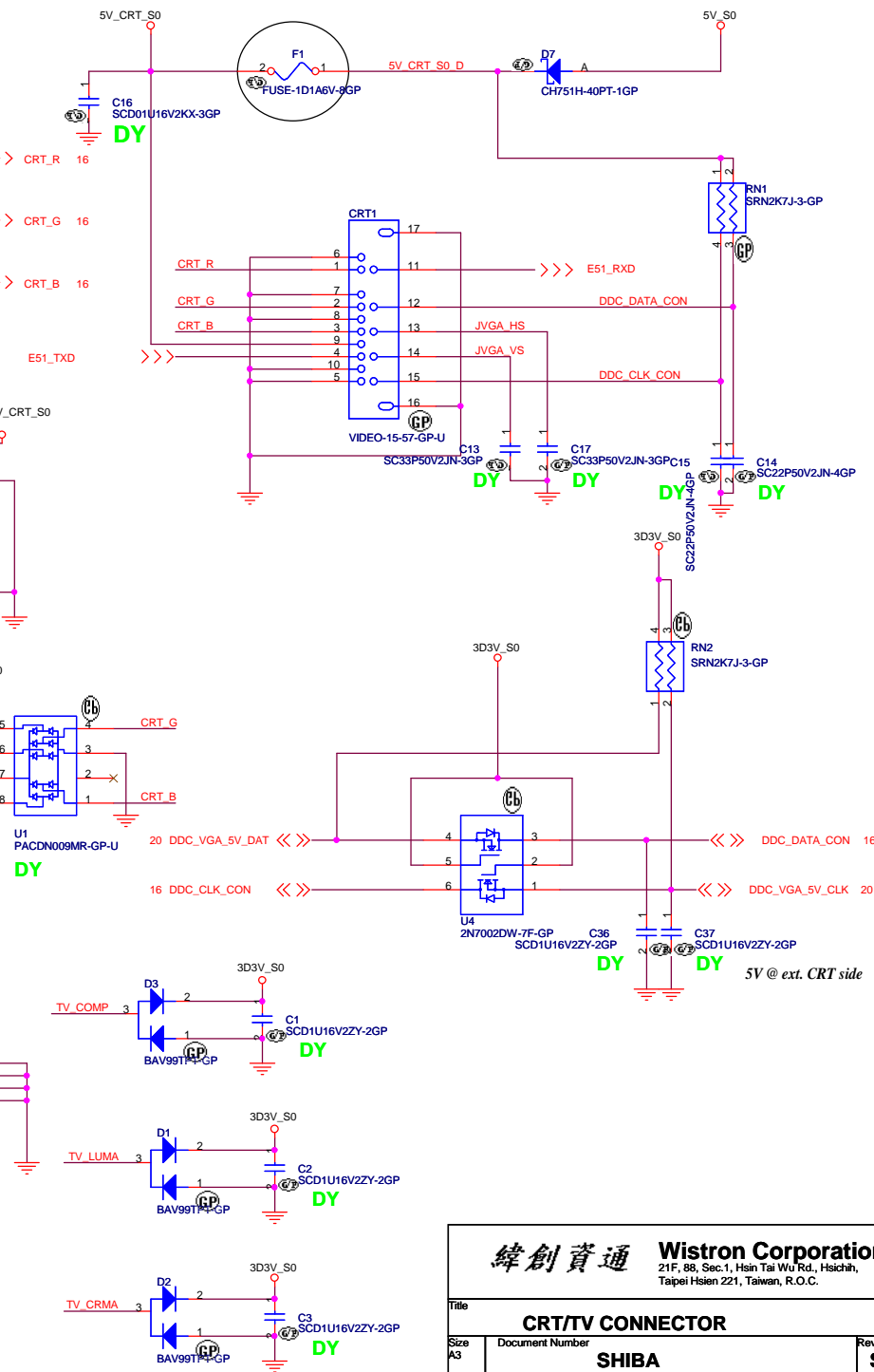
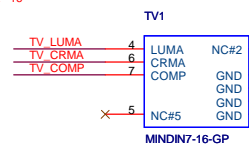


TV OUT CONN

Layout Note:
Place this 2 resistors
close to the TV-out
connector



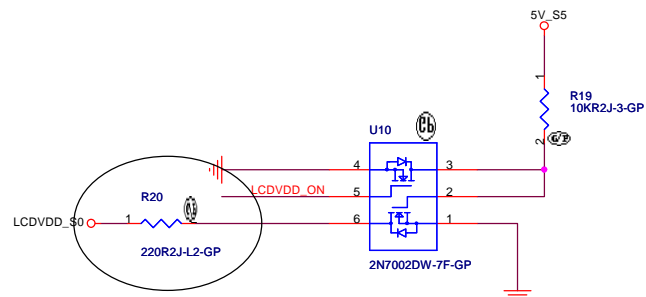
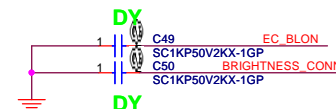
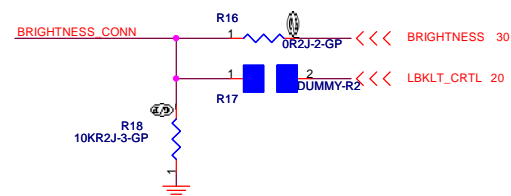
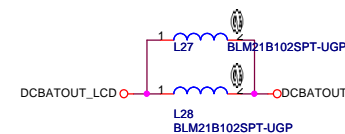
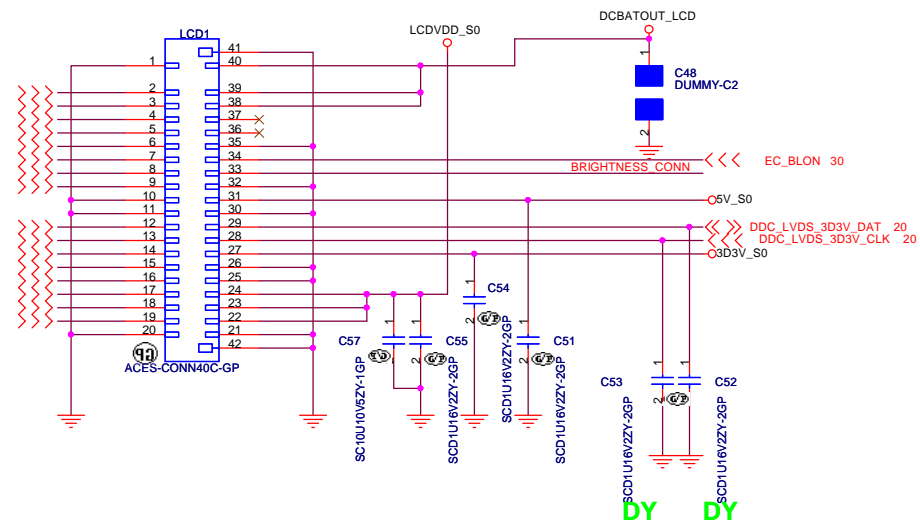
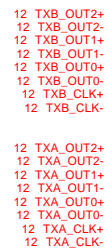
Thr org part is 68.2703N.10B



緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

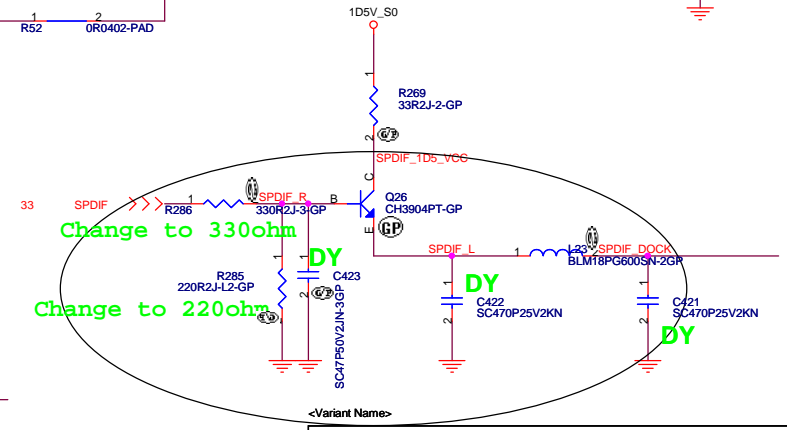
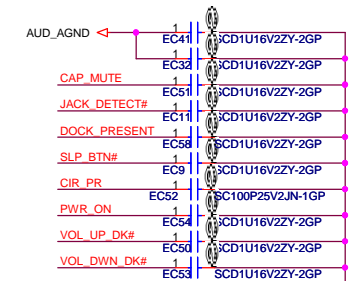
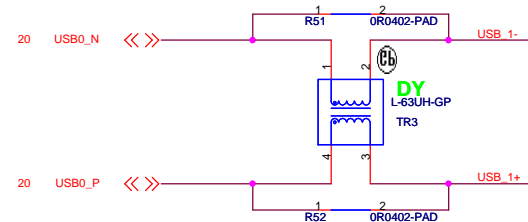
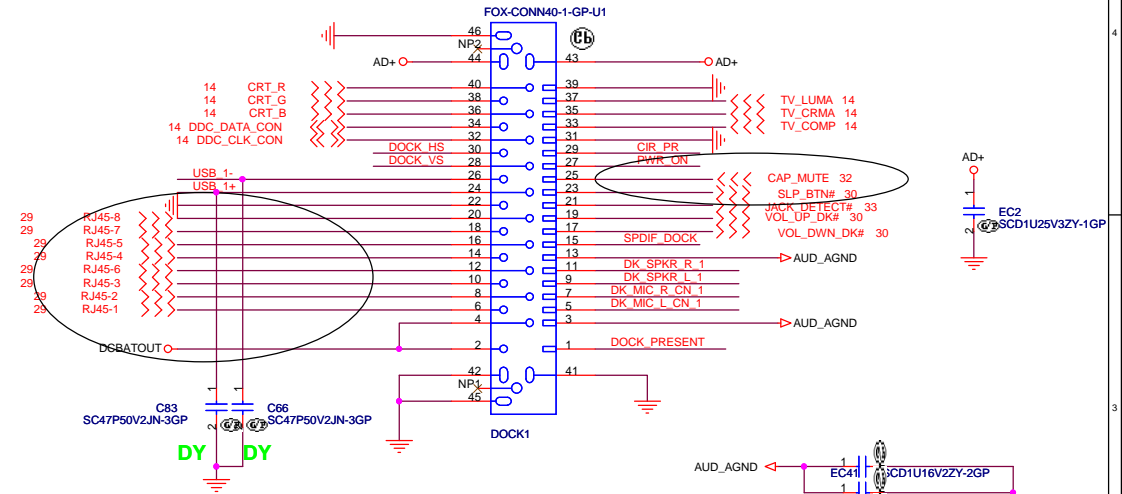
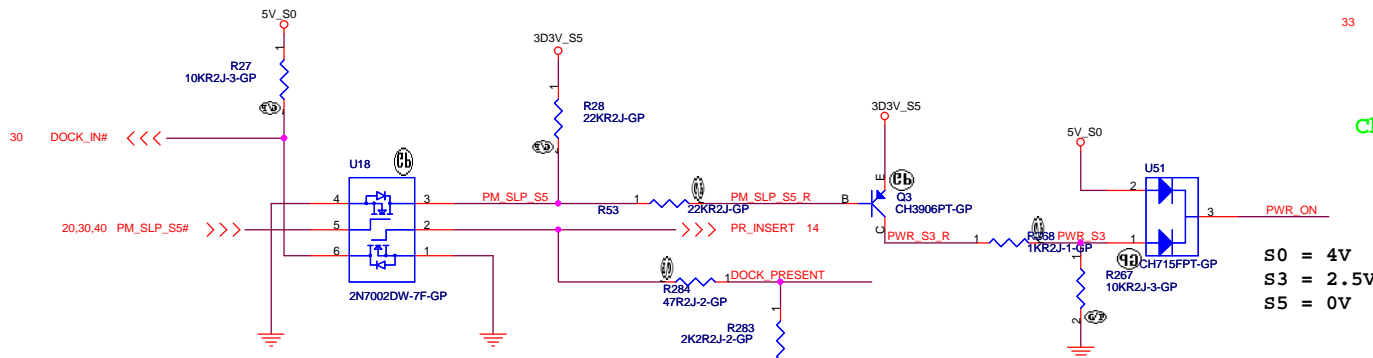
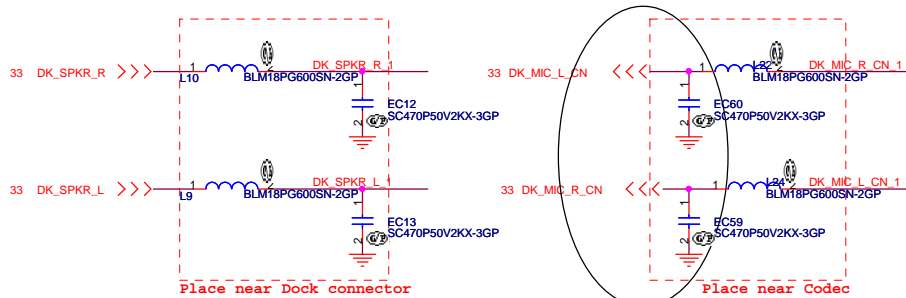
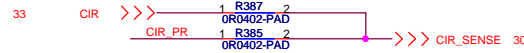
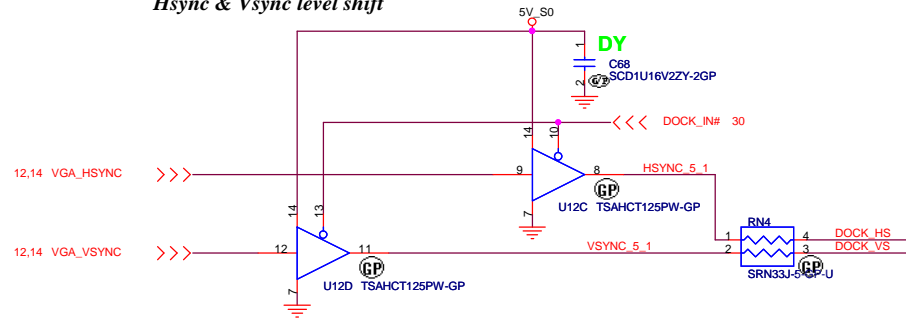
CRT/TV CONNECTOR		
Size A3	Document Number SHIBA	Rev SA
Date: Thursday, February 23, 2006	Sheet 14 of 44	



 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
LCD/Inverter Connector	
Size Custom	Document Number SHIBA
Date: Friday, February 24, 2006	Sheet 15 of 44 SA

Docking Connector

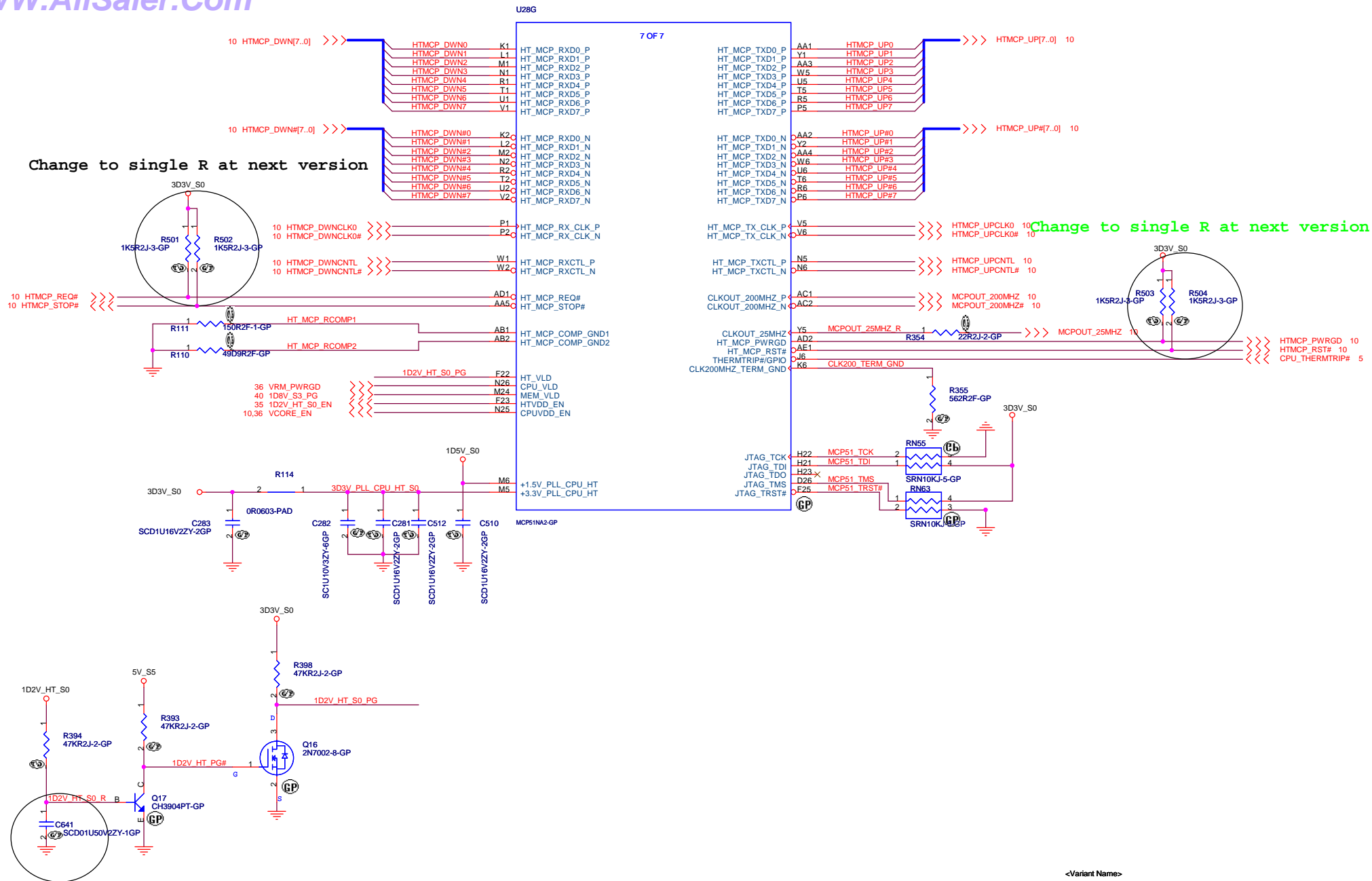
Hsync & Vsync level shift



S0 = 4V
S3 = 2.5V
S5 = 0V

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Board to board conn/ Docking			
Title	Document Number	Rev	SA
Size	A3	SHIBA	
Date:	Monday, February 27, 2006	Sheet	16 of 44



25 PCI_AD[0..31] <<<>

U28A

1 OF 7

PCI_AD0	AF19	PCI_AD0
PCI_AD1	AB21	PCI_AD1
PCI_AD2	AC19	PCI_AD2
PCI_AD3	AA20	PCI_AD3
PCI_AD4	AA19	PCI_AD4
PCI_AD5	AE20	PCI_AD5
PCI_AD6	AE19	PCI_AD6
PCI_AD7	AE20	PCI_AD7
PCI_AD8	AB20	PCI_AD8
PCI_AD9	AB19	PCI_AD9
PCI_AD10	AA18	PCI_AD10
PCI_AD11	AB18	PCI_AD11
PCI_AD12	AE18	PCI_AD12
PCI_AD13	AF18	PCI_AD13
PCI_AD14	AC17	PCI_AD14
PCI_AD15	AA17	PCI_AD15
PCI_AD16	AB15	PCI_AD16
PCI_AD17	AE15	PCI_AD17
PCI_AD18	AE15	PCI_AD18
PCI_AD19	AF14	PCI_AD19
PCI_AD20	AE14	PCI_AD20
PCI_AD21	AA14	PCI_AD21
PCI_AD22	AC13	PCI_AD22
PCI_AD23	AB13	PCI_AD23
PCI_AD24	AB13	PCI_AD24
PCI_AD25	AE13	PCI_AD25
PCI_AD26	AE13	PCI_AD26
PCI_AD27	AA12	PCI_AD27
PCI_AD28	AB12	PCI_AD28
PCI_AD29	AE12	PCI_AD29
PCI_AD30	AE12	PCI_AD30
PCI_AD31	AE11	PCI_AD31

25 PCI_C/BE#0	<<<>	AD19	PCI_CBE#0
25 PCI_C/BE#1	<<<>	AB17	PCI_CBE#1
25 PCI_C/BE#2	<<<>	AA15	PCI_CBE#2
25 PCI_C/BE#3	<<<>	AA13	PCI_CBE#3

25 PCI_FRAME#	<<<>	AC15	PCI_FRAME#
25 PCI_IRDY#	<<<>	AD15	PCI_IRDY#
25 PCI_TRDY#	<<<>	AB16	PCI_TRDY#
25 PCI_STOP#	<<<>	AE16	PCI_STOP#
25 PCI_DEVSEL#	<<<>	AA16	PCI_DEVSEL#
25 PCI_PAR	<<<>	AE17	PCI_PAR
25 PCI_PERR#	<<<>	AE17	PCI_PERR#/GPIO
25 PCI_SERR#	<<<>	AD11	PCI_SERR#
25,30 PM_CLKRUN#	<<<>	AE25	PCI_PME#/GPIO

25 PCIRST#	<<<>	PCIRST# R	AE25	PCI_RESET#0
24 PCIRST#_IDE	<<<>	PCIRST#_IDE R	AD24	PCI_RESET#1
29 PCIRST#_NEW	<<<>	PCIRST#_NEW R	AE26	PCI_RESET#2
30,31 LPC_RST#	<<<>	LPC_RST# R	L26	PCI_RESET#3

MCP51NA2-GP

PCI_REQ#0	AA22	PCI_REQ#0	<<<>	PCI_REQ#0	25
PCI_REQ#1	AE22	PCI_REQ#1	<<<>	PCI_REQ#1	25
PCI_REQ#2	AE21	PCI_REQ#2	<<<>	PCI_REQ#2	25
PCI_REQ#3/GPIO	AE22	PCI_REQ#3	<<<>	PCI_REQ#3	25
PCI_REQ#4/GPIO	AE23	PCI_REQ#4	<<<>	PCI_REQ#4	25

PCI_GNT#0	AE21	PCI_GNT#0	>>>>	PCI_GNT#0	25
PCI_GNT#1	AC21	PCI_GNT#1	>>>>	PCI_GNT#1	25
PCI_GNT#2	AA21	PCI_GNT#2	>>>>	PCI_GNT#2	25
PCI_GNT#3/GPIO	AB24	PCI_GNT#3	>>>>	PCI_GNT#3	25
PCI_GNT#4/GPIO	AB24	PCI_GNT#4	>>>>	PCI_GNT#4	25

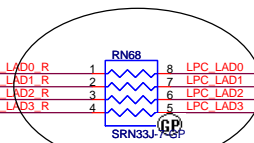
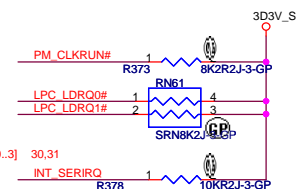
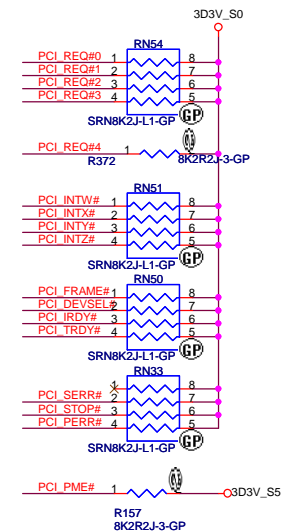
PCI_INTW#	AE11	PCI_INTW#	>>>>	PCI_INTW#	25
PCI_INTX#	AB11	PCI_INTX#	>>>>	PCI_INTX#	25
PCI_INTY#	AC11	PCI_INTY#	>>>>	PCI_INTY#	25
PCI_INTZ#	AA11	PCI_INTZ#	>>>>	PCI_INTZ#	25

PCI_CLK0	AE24	PCI_CLK R	>>>>	PCI_CLK	25
PCI_CLK1	AE24	PCI_CLK1 R	>>>>	PCI_CLK	25
PCI_CLK2	AE24	PCI_CLK2 R	>>>>	PCI_CLK	25
PCI_CLK3	AB23	PCI_CLK3 R	>>>>	PCI_CLK	25
PCI_CLK4	AB23	PCI_CLK4 R	>>>>	PCI_CLK	25
PCI_CLKIN	AC23	PCI_CLKIN	>>>>	PCI_CLK	25

LPC_AD0	K24	LPC_LAD0 R	>>>>	LPC_LAD0	30,31
LPC_AD1	H26	LPC_LAD1 R	>>>>	LPC_LAD1	30,31
LPC_AD2	H25	LPC_LAD2 R	>>>>	LPC_LAD2	30,31
LPC_AD3	K22	LPC_LAD3 R	>>>>	LPC_LAD3	30,31

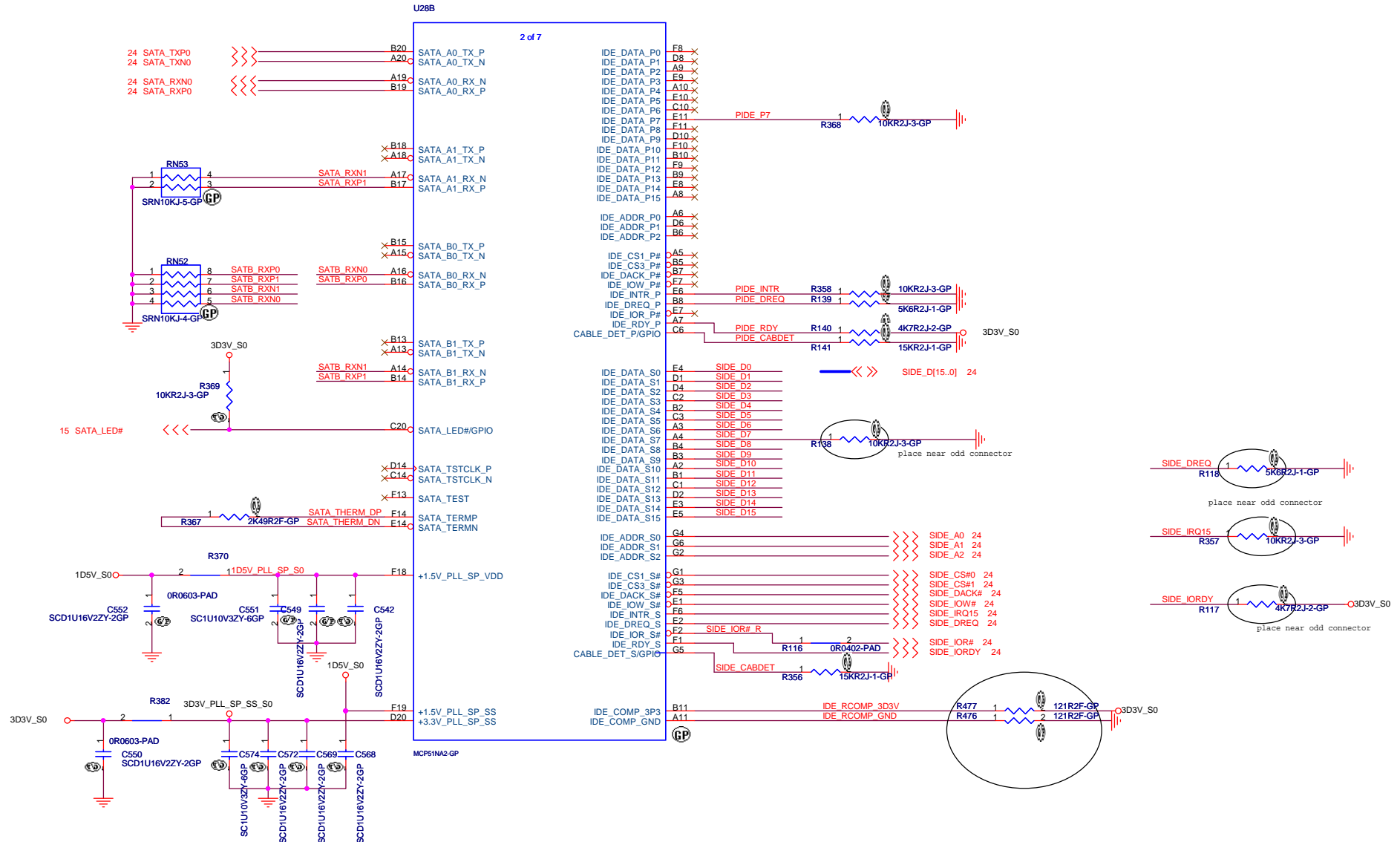
LPC_FRAME#	G25	LPC_LDRQ#	>>>>	LPC_LFRAME#	30,31
LPC_DRQ#0	K21	LPC_LDRQ#	>>>>	LPC_LFRAME#	30,31
LPC_DRQ#1/LPC_CS#	K23	LPC_LDRQ1#	>>>>	LPC_LFRAME#	30,31
LPC_SERIRQ	L22	LPC_SERIRQ	>>>>	INT_SERIRQ	25,30
LPC_PWRDWN#/GPIO	H24	LPC_PWRDWN#	>>>>	INT_SERIRQ	25,30

LPC_CLK0	F26	LPC_CLK R	>>>>	LPC_CLK	30
LPC_CLK1	G26	PCI_CLK1 R	>>>>	PCI_CLK_GOLD	31



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
MCP51(2/6)PCI		
Size	Document Number	Rev
A3	SHIBA	SA
Date	Monday, February 20, 2006	Sheet 18 of 44



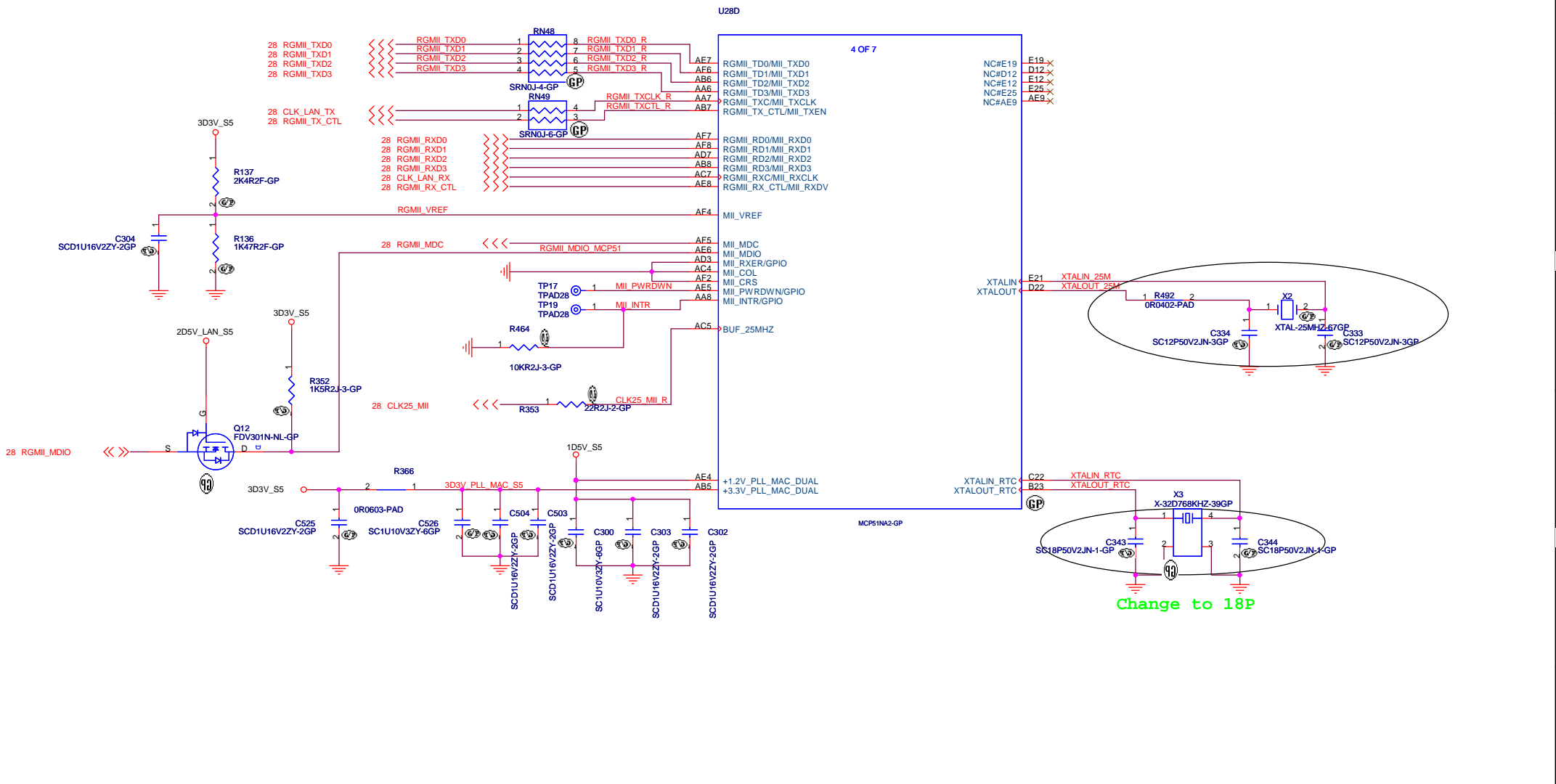


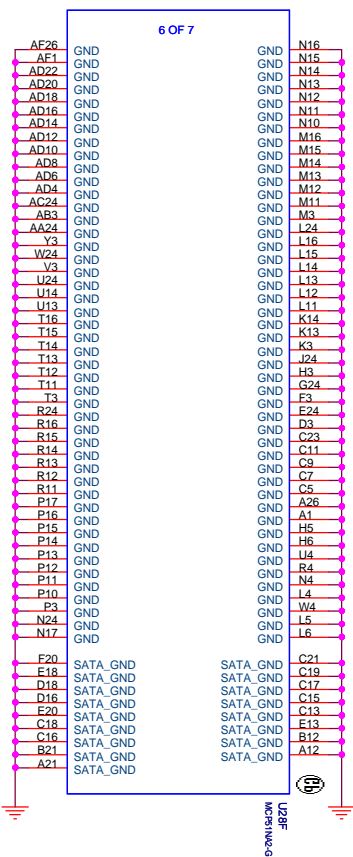
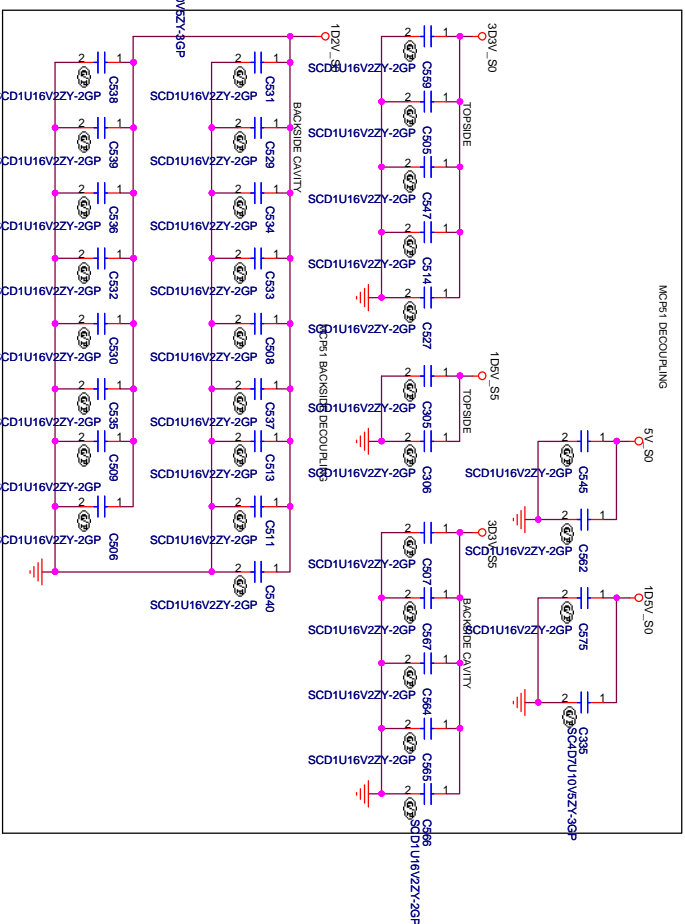
D

C

B

A



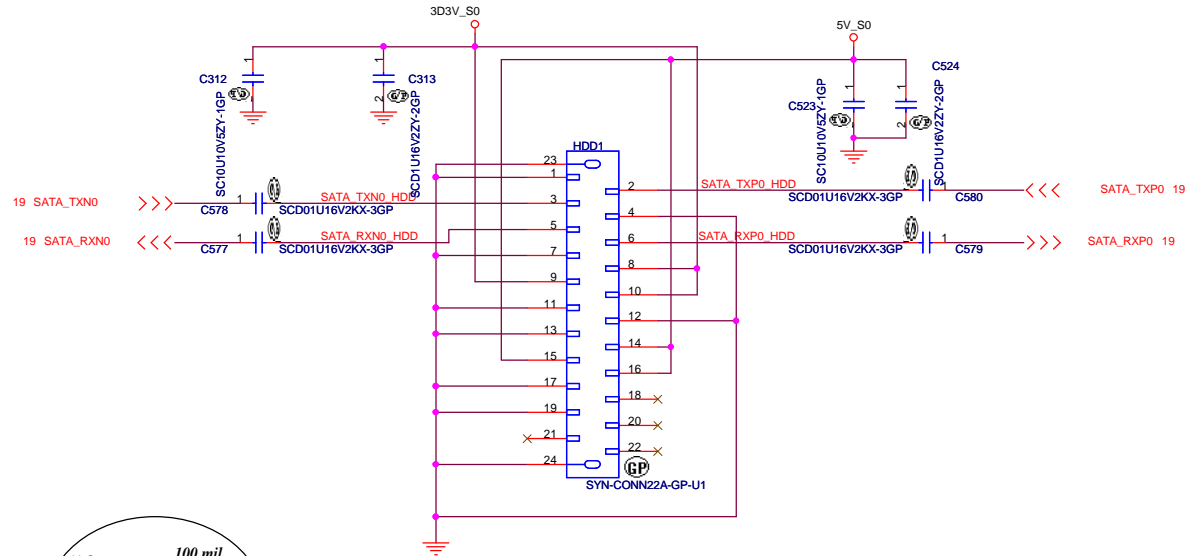


<Variant Name>	
<p>緯創實通</p> <p>Wistron Corporation</p> <p>2/F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipai Hsien Z21, Taiwan, R.O.C.</p>	
Title	MCPS1(6/6)POWER
Size	Document Number
A3	SHIBA
date - Monday, February 20, 2006	Sheet 22 of 44
	Rev SB

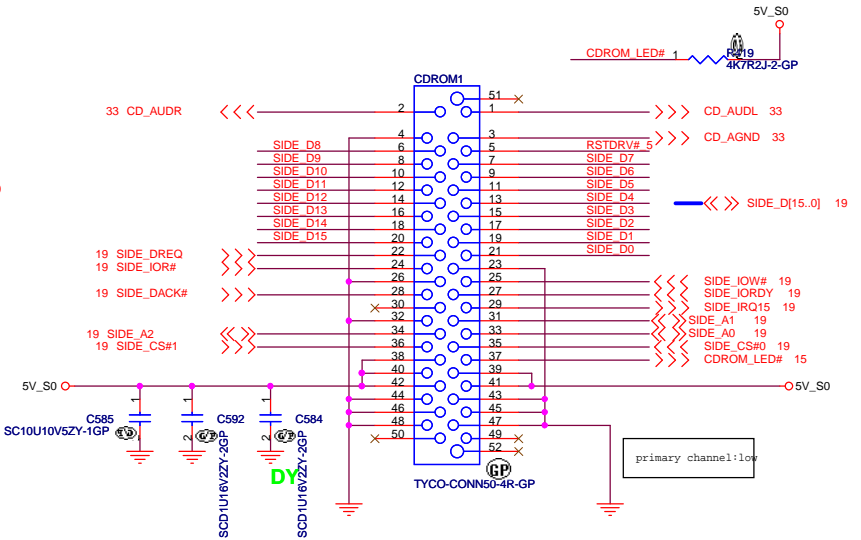


Title			
Thermal/Fan Controller			
Size	Document Number	Rev	
Custom	SHIBA	SA	
Date:	Monday, February 20, 2006	Sheet	23 of 44

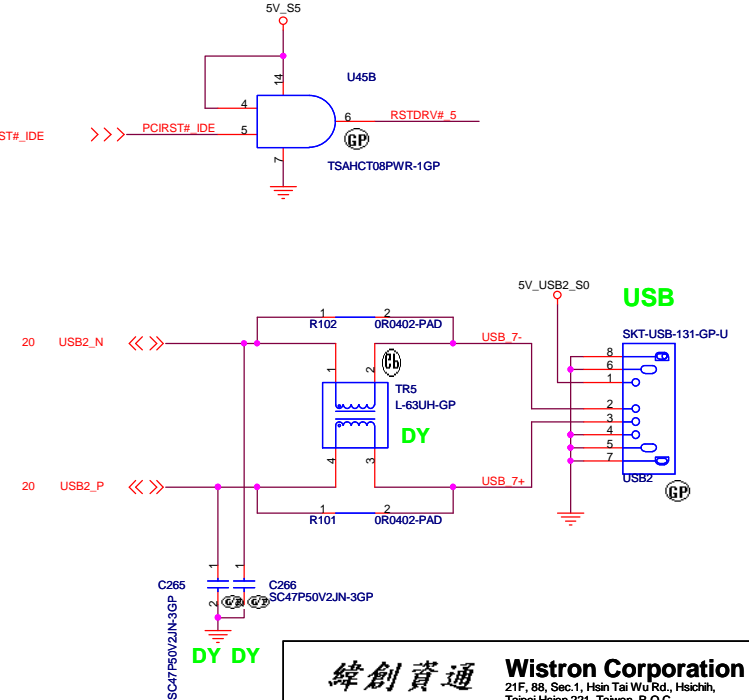
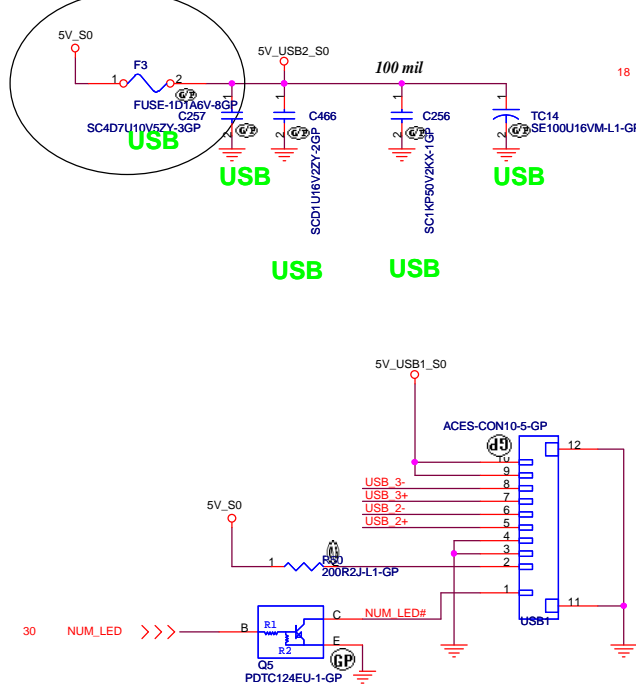
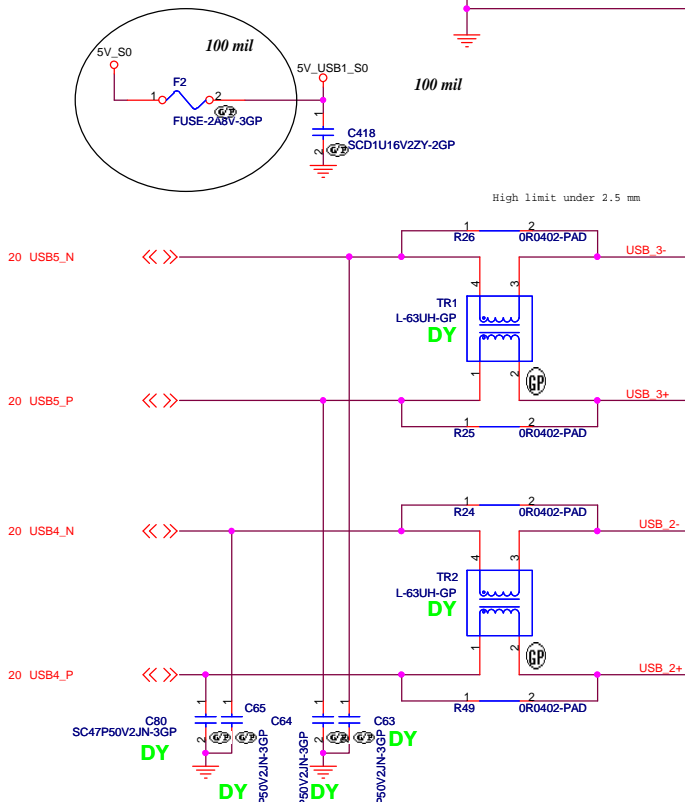
SATA HD Connector



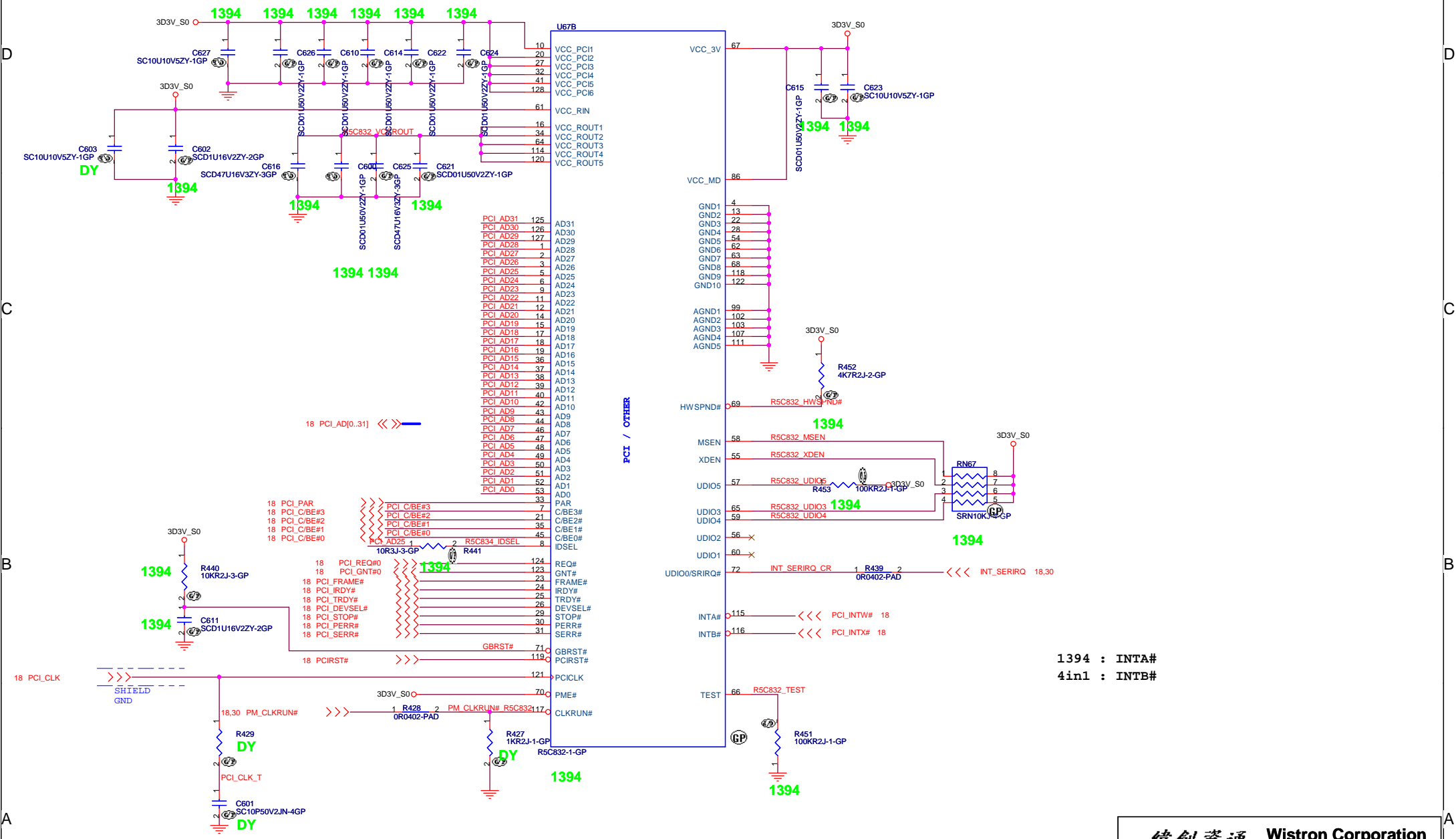
CD-ROM CONNECTOR



USB PORT

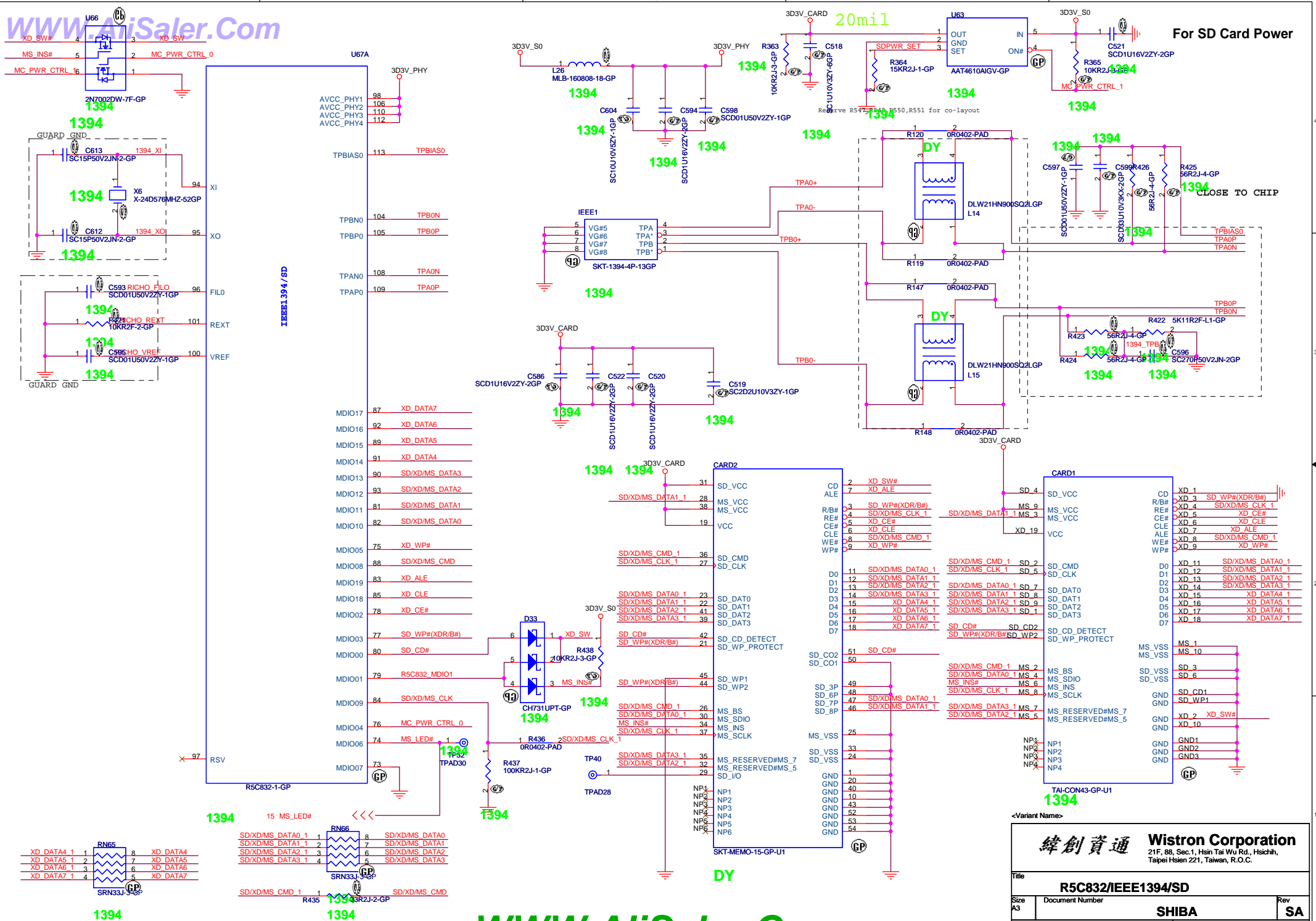


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	HD/CDROM		
Size	Document Number	Rev	
A3	SHIBA	SA	
Date:	Saturday, March 04, 2006	Sheet	24 of 44



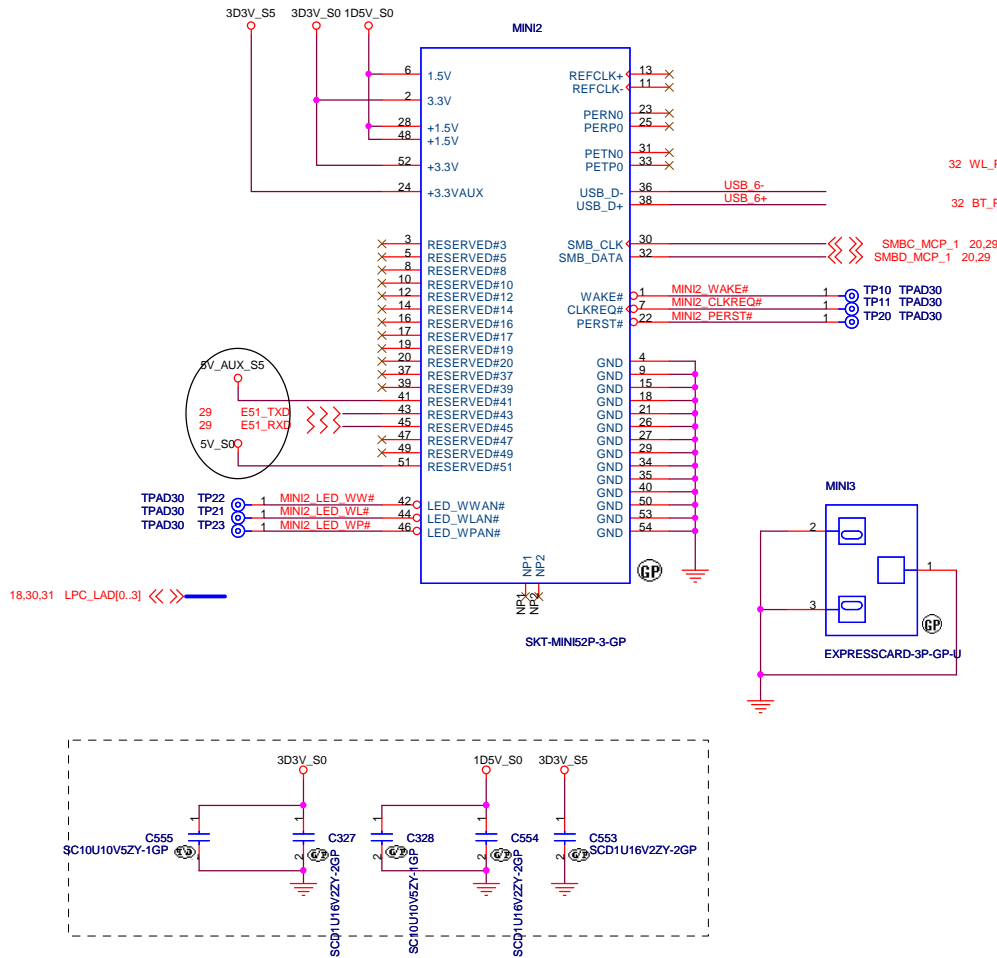
1394 : INTA#
4in1 : INTB#

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: R5C832/PCI			
Size A3	Document Number	SHIBA	Rev SA
Date: Monday, February 20, 2006	Sheet 25	of	44

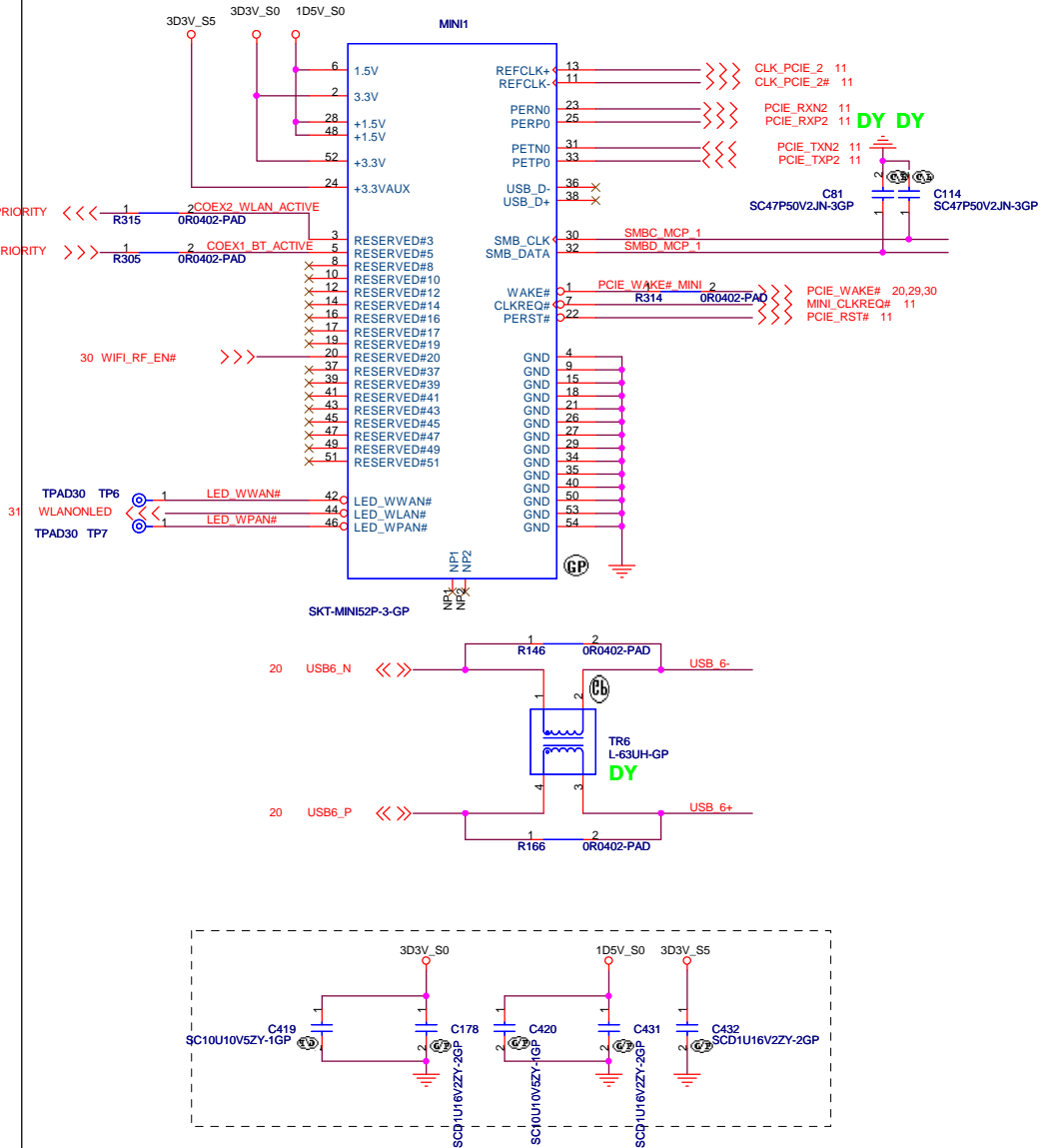


Mini Card Connector

Mini Card Connector 1



Mini Card Connector 2



緯創資通

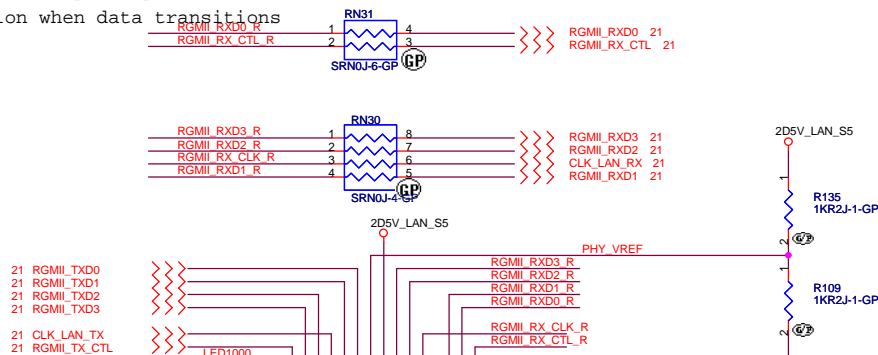
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

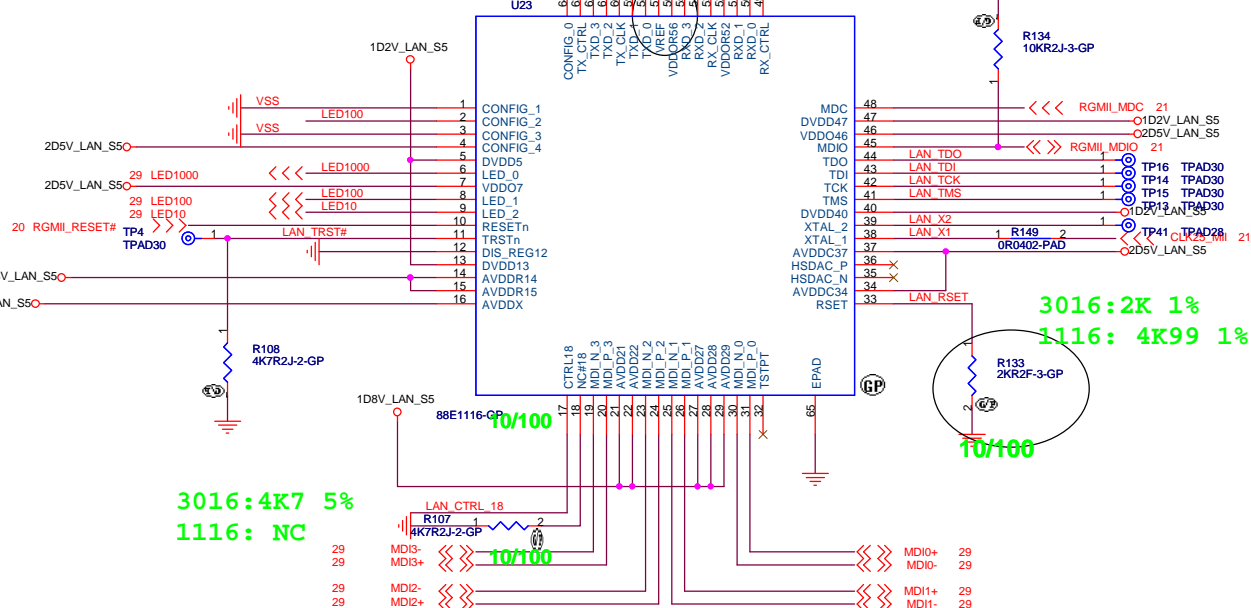
Title			MINI CARD CONN .
Size	Document Number	Rev	SA
A3	SHIBA		
Date:	Thursday, February 23, 2006	Sheet	27 of 44

1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities

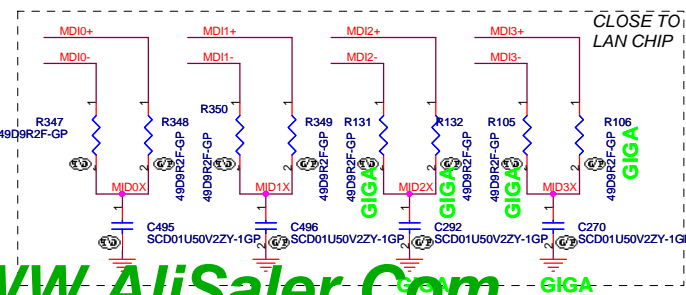
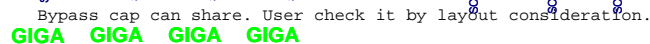
```
Put L10 for E3016
application since
pin 28
NOB for E1116
```



```
3016: 71.88316.A03
1116: 71.88116.A03
```



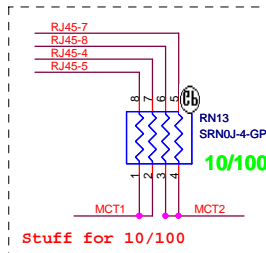
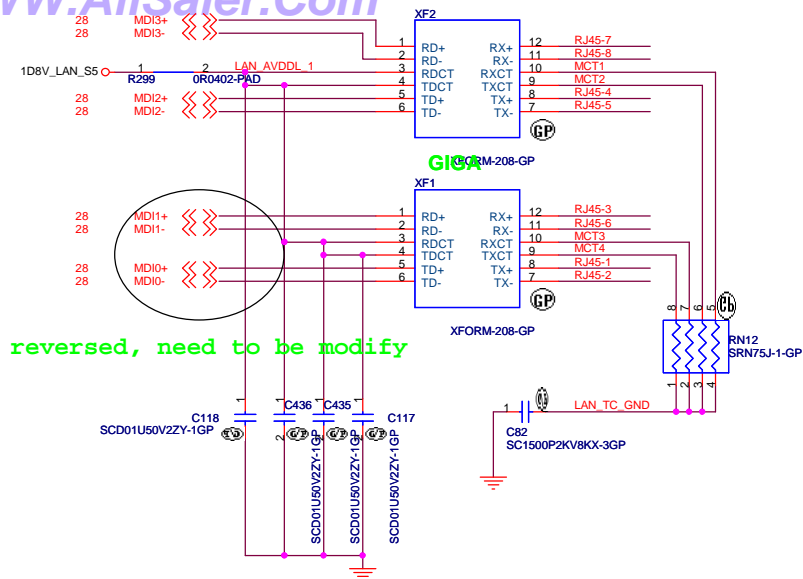
```
3016:4K7  5%
1116:  NC
```



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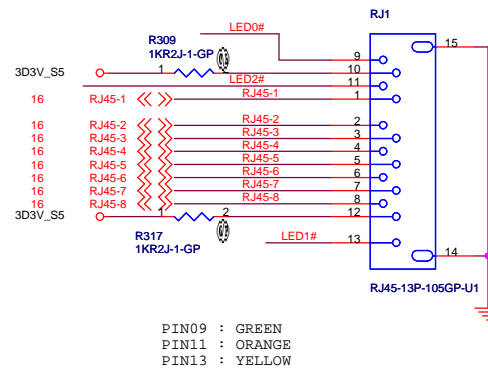
Rev
SA

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1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

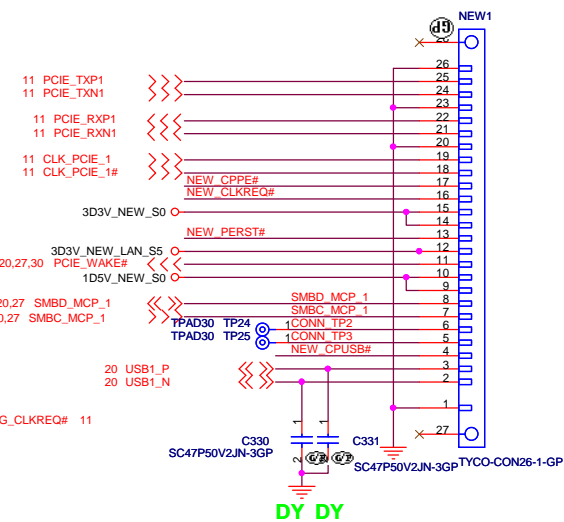
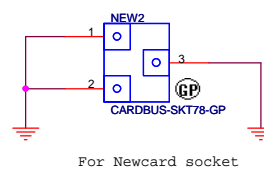
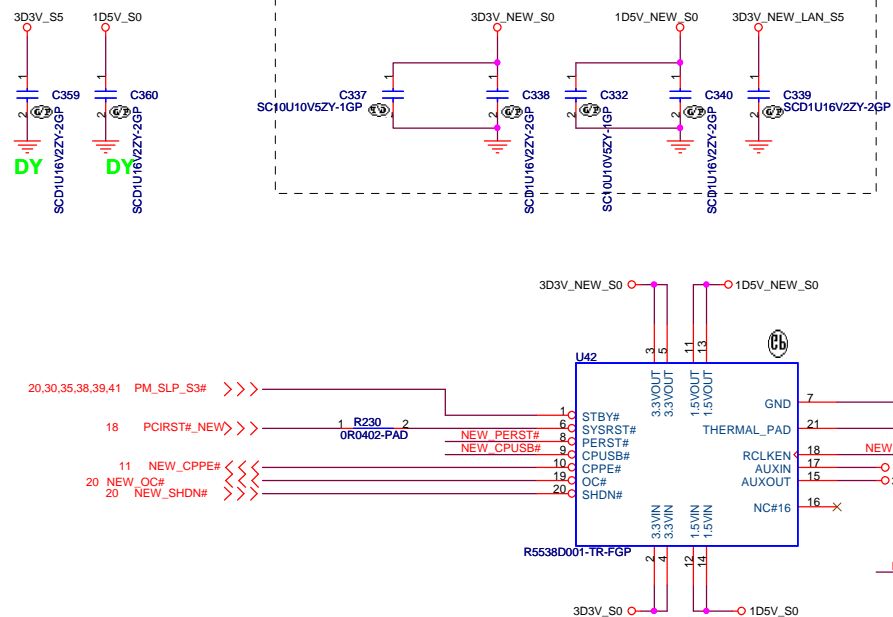
```
GREEN: LINK 10/100 Mbps
YELLOW: TX/RX ACTIVITY
ORANGE: LINK 1000Mbps
```



NEWCARD Connector

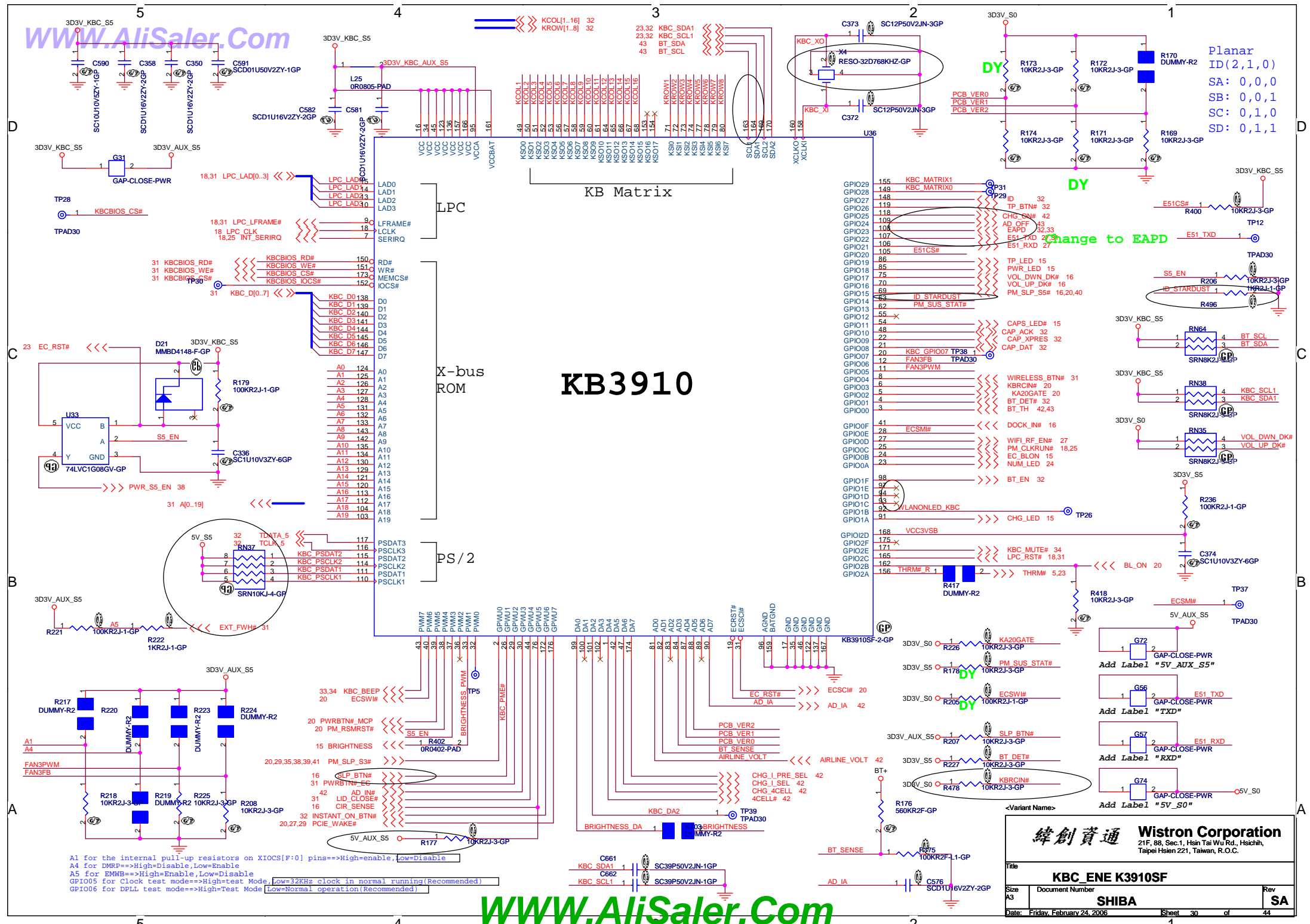
Place them Near to Chip

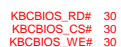
Place them Near to Connector



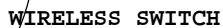
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
New Card			
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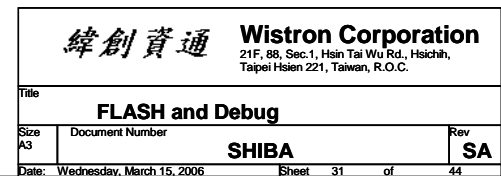
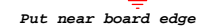




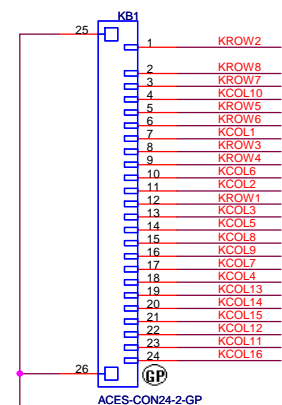
POWER SWITCH



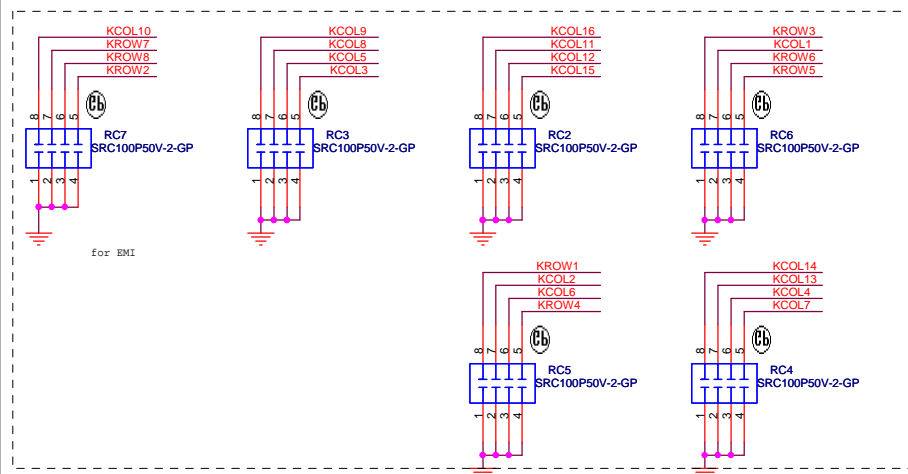
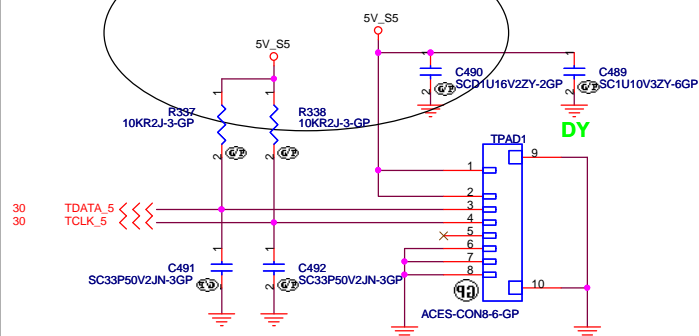
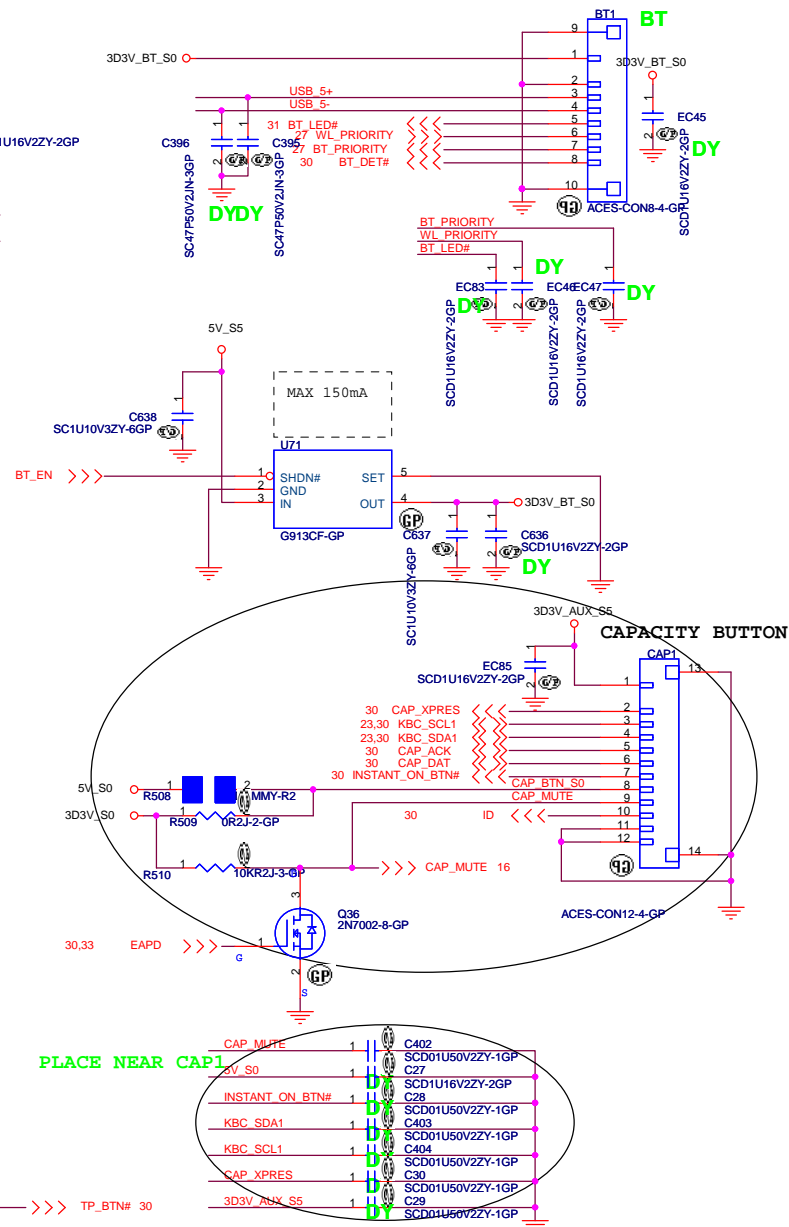
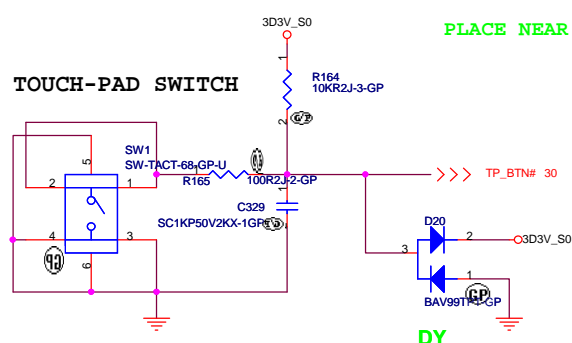
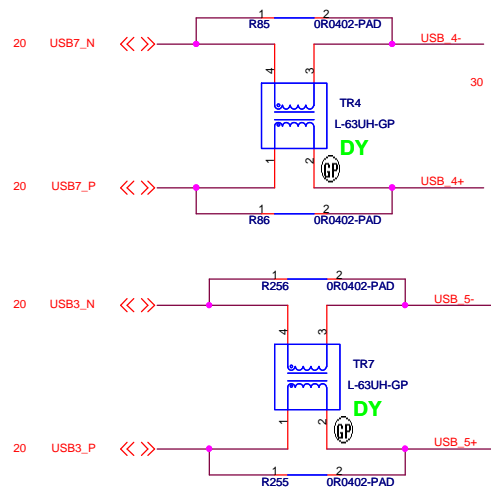
(BOTTOM VIEW)



Blue thumb



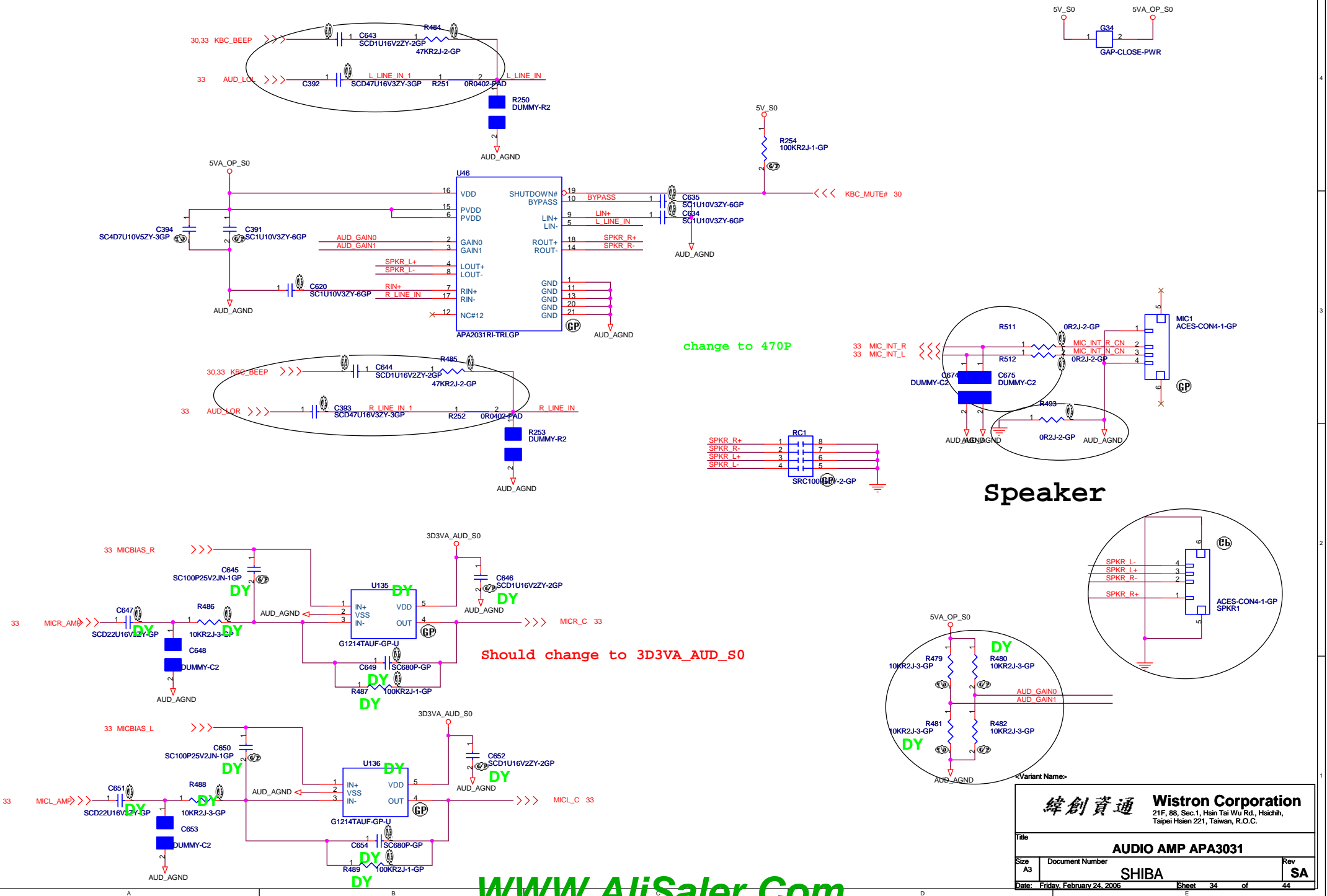
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

[illegible]

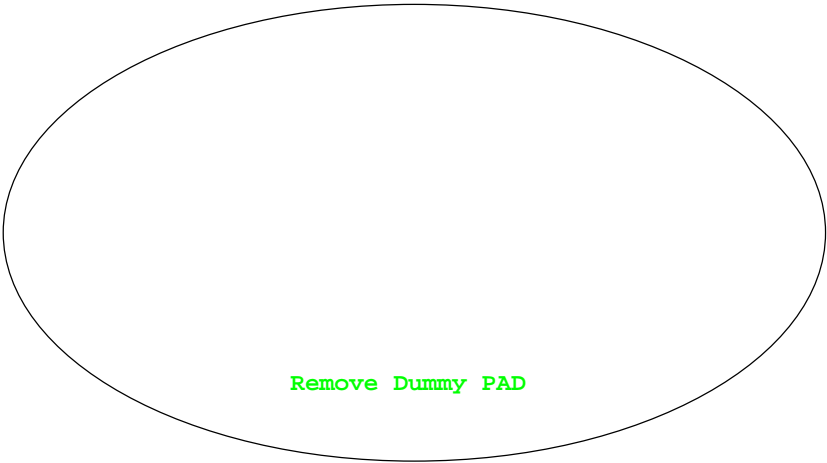
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
KeyBoard-CONN		
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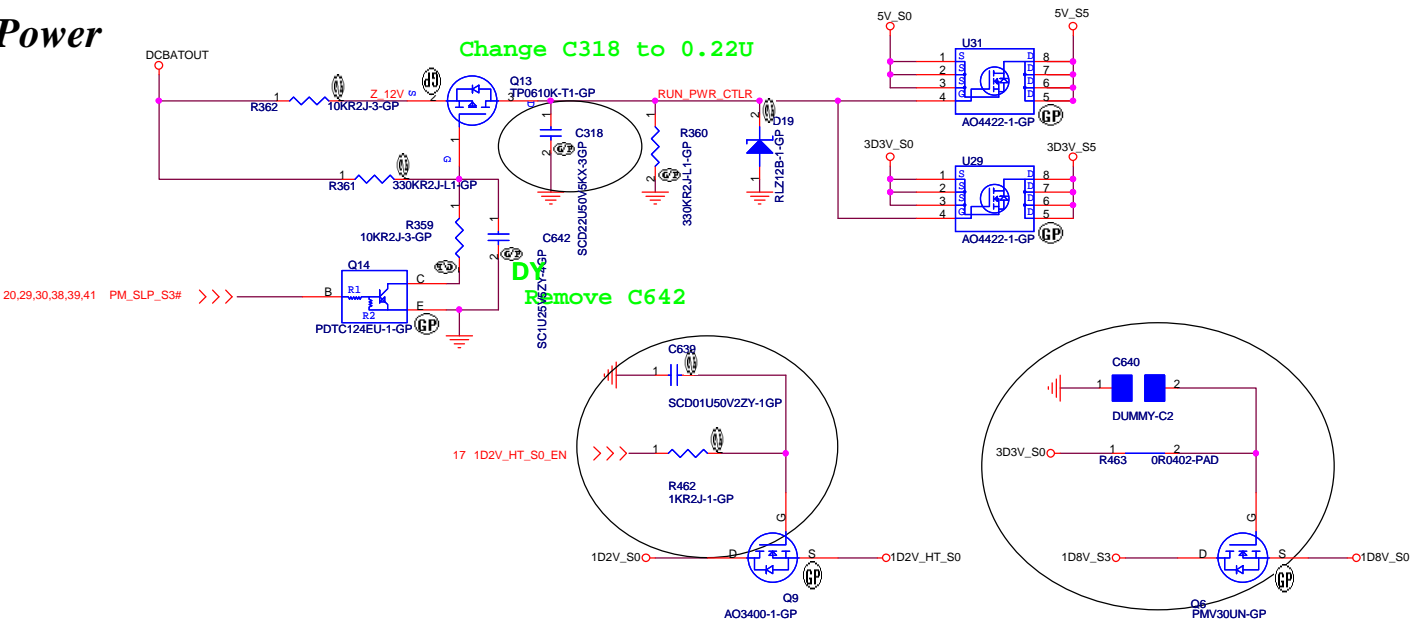




Suspend Power



Run Power



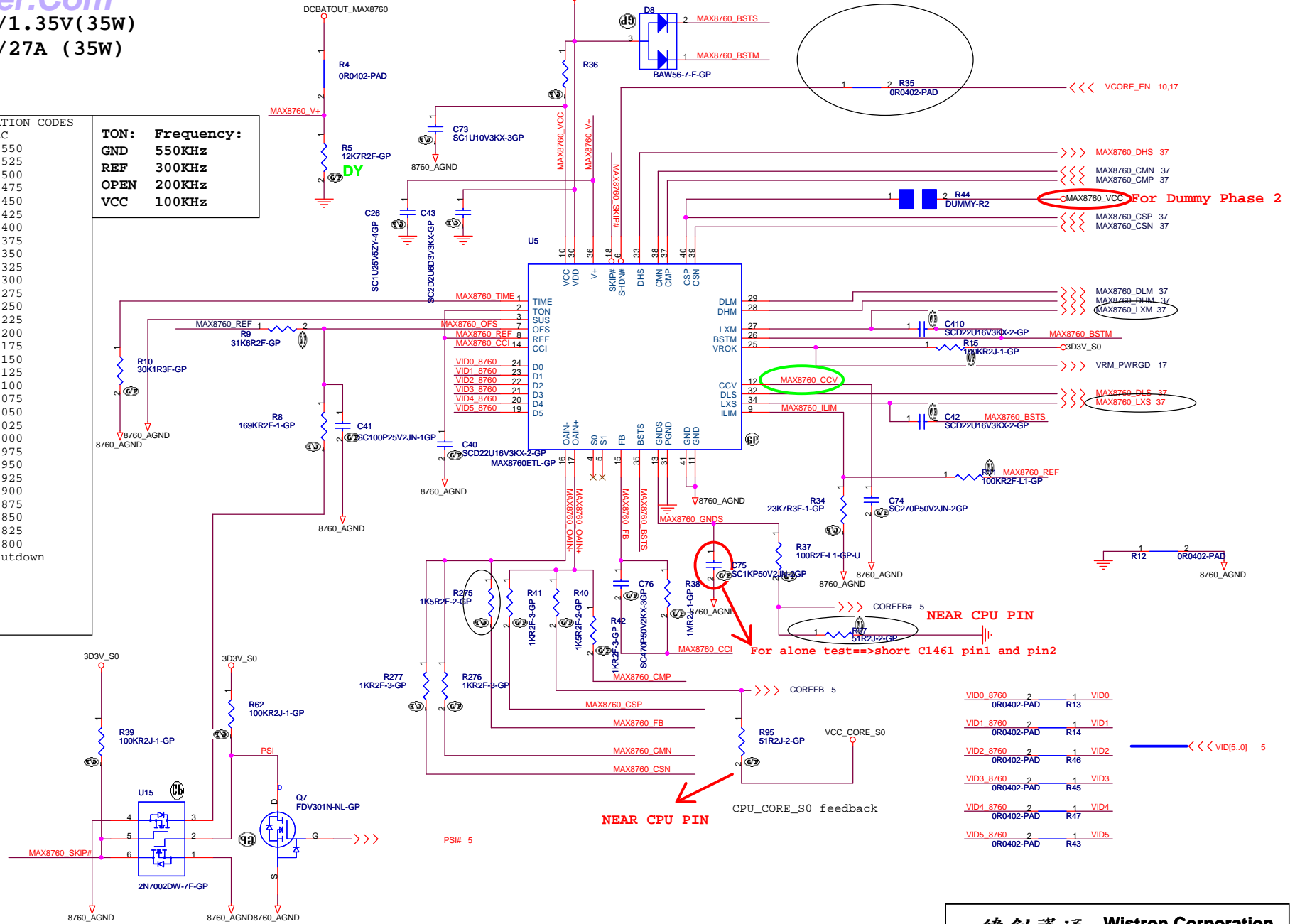
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
PWRPLANE&RESETLOGIC			
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WWW.AliSaler.Com
CPU_VCORE
VID=1.20V(25W)/1.35V(35W)
Iomax=21A(25W)/27A (35W)
OCP=40A~45A

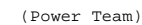
TABLE 1. VOLTAGE IDENTIFICATION CODES

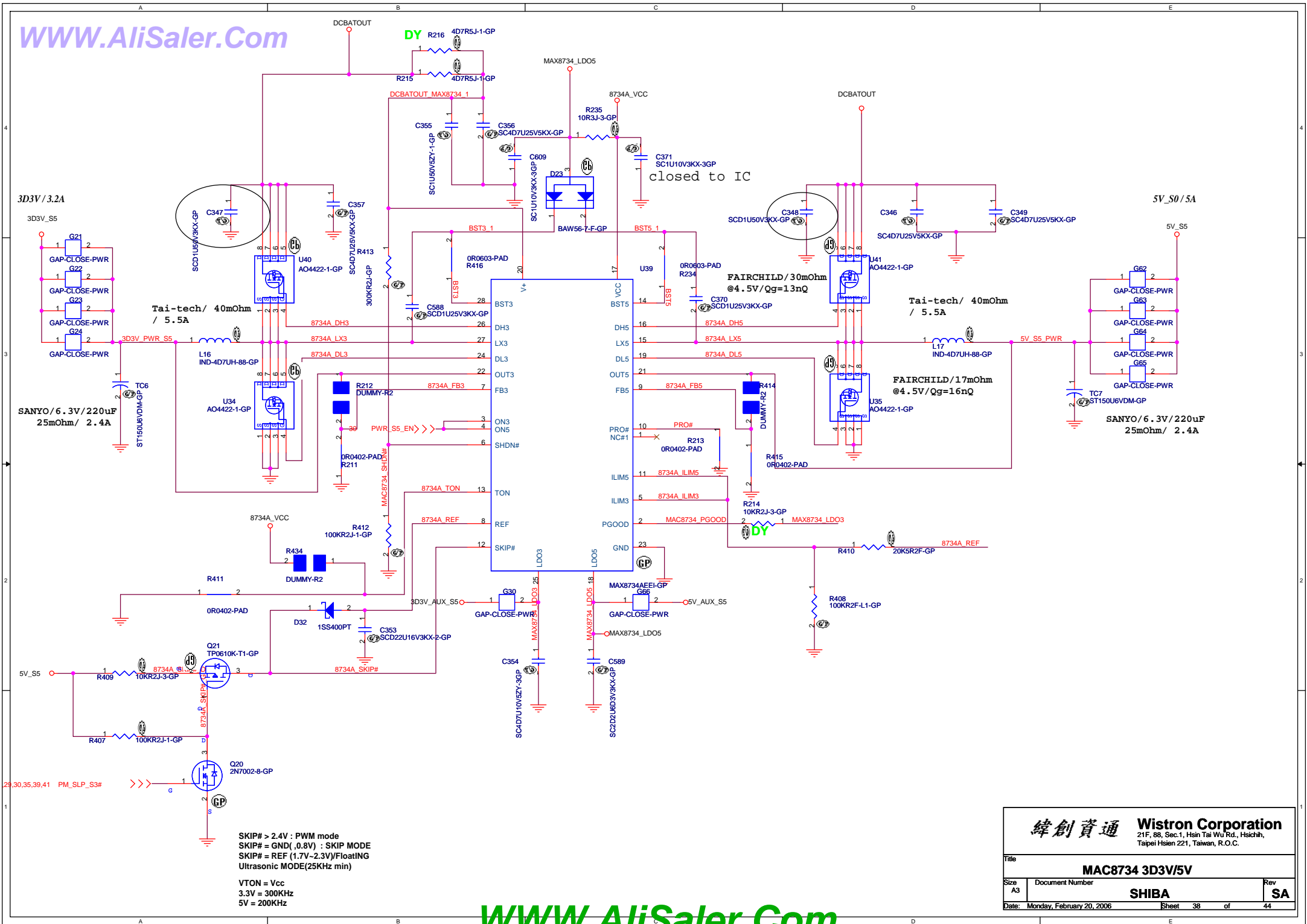
VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

TON: Frequency:
GND 550KHz
REF 300KHz
OPEN 200KHz
VCC 100KHz



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Title CPU CORE MAX8760(1/2)	
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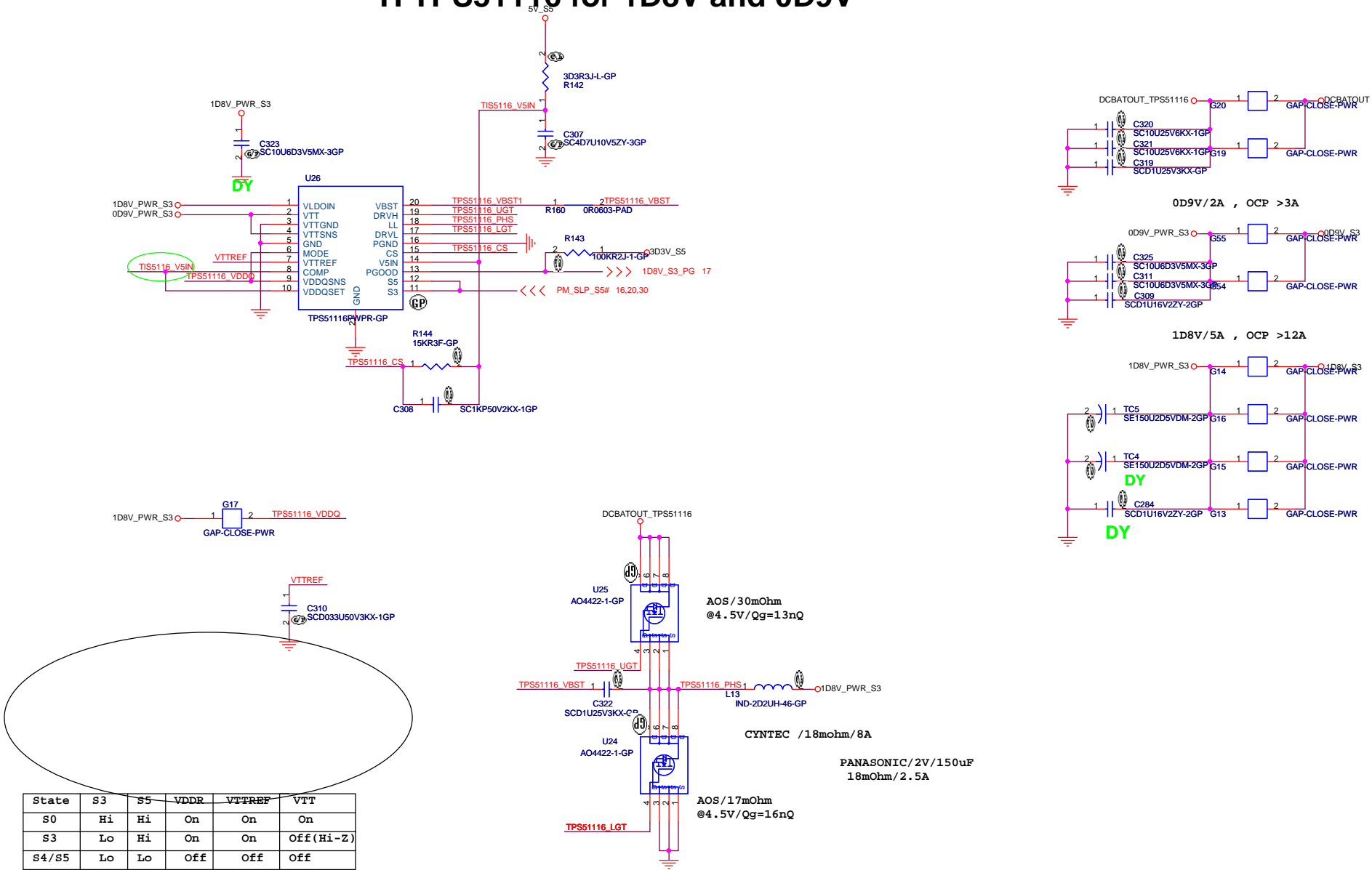
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			MAC8734 3D3V/5V	
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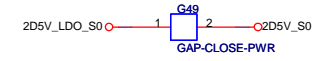
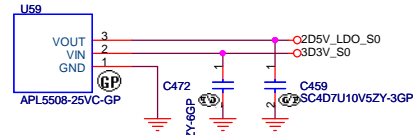
A

A

TI TPS51116 for 1D8V and 0D9V

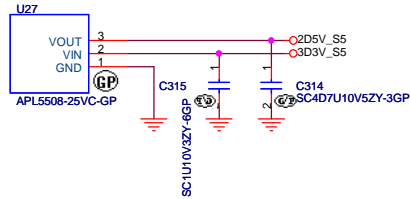
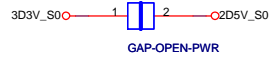


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

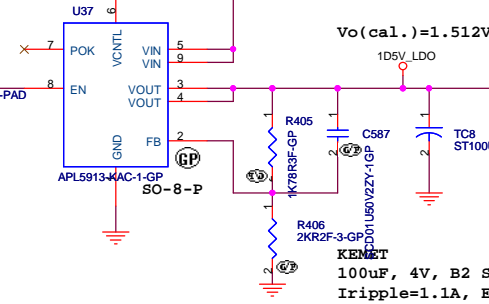
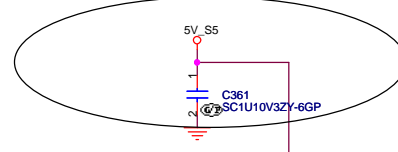


20,29,30,35,38,39 PM_SLP_S3#

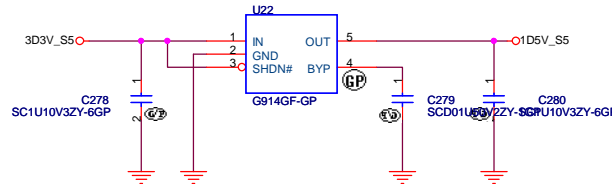
G50



Change to S5 power plane



$$V_o = 0.8 * (1 + (R1/R2))$$



2nd source : 74.00916.D3F

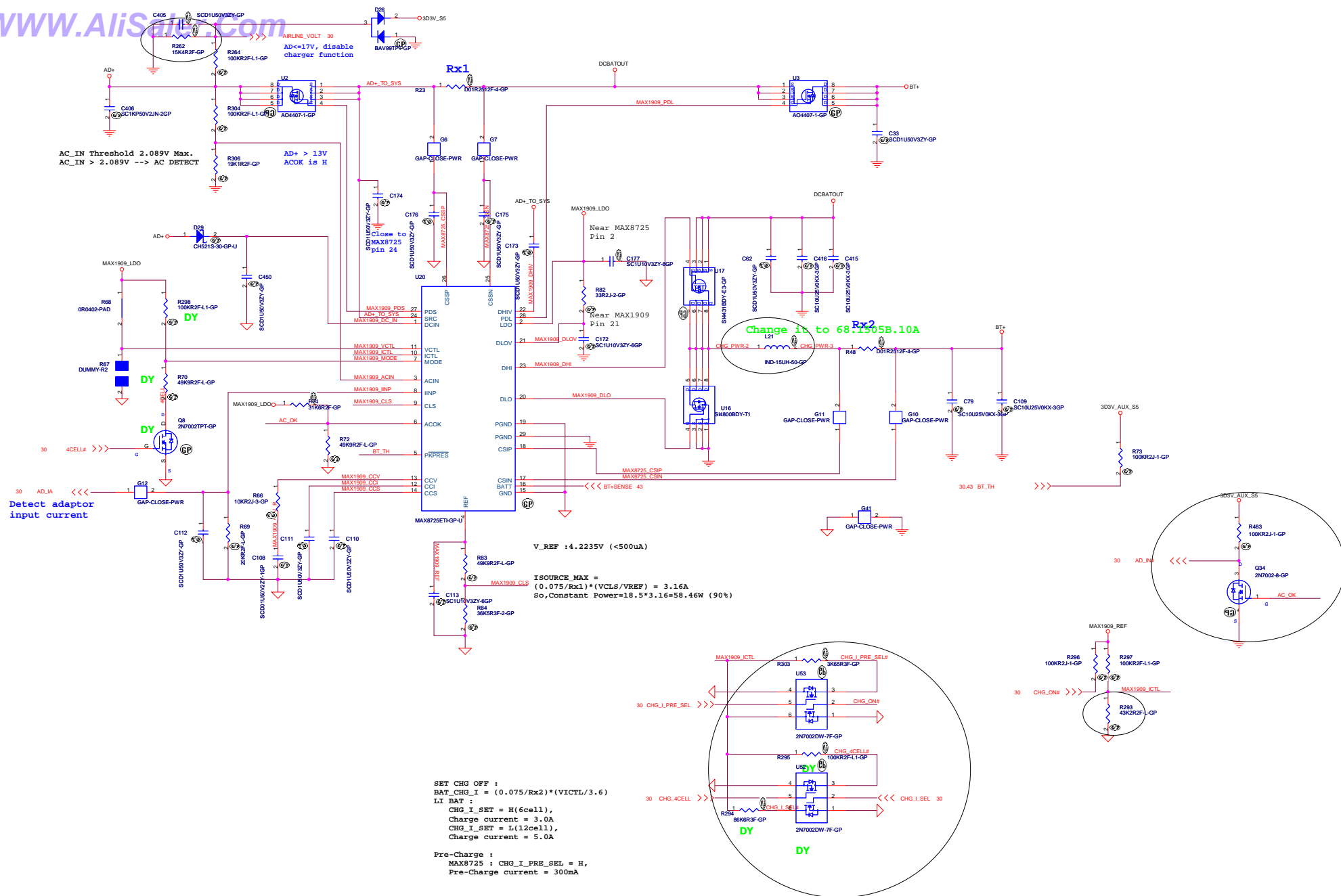
Vo(cal.)=1.512V

1D5V_S0
Iomax=1.3A
OCP=2.6A

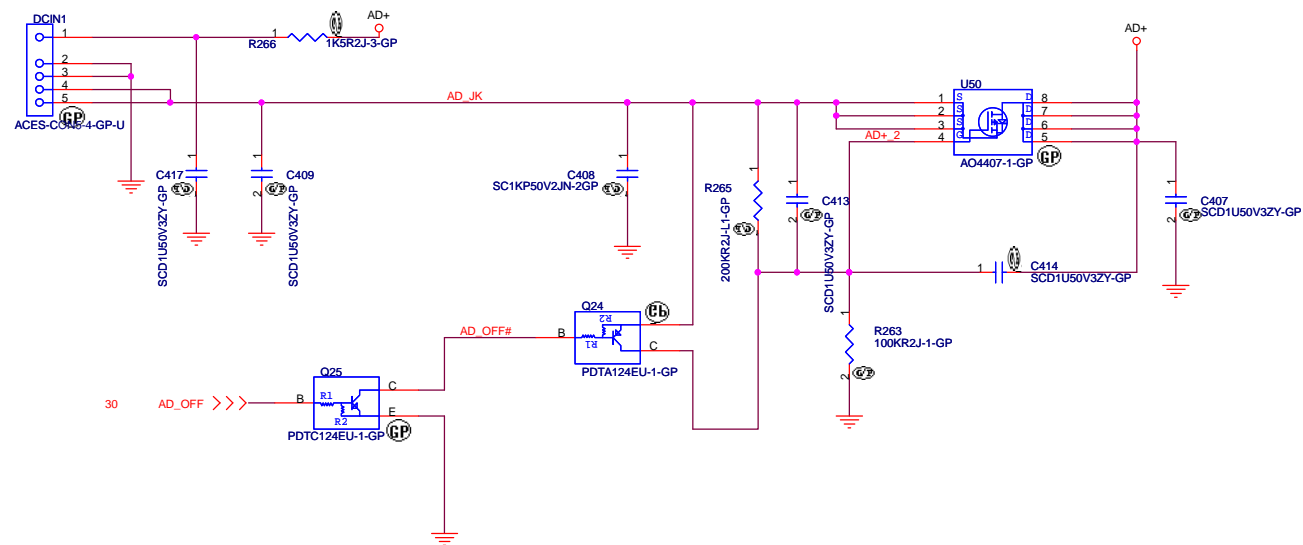
Trace Length=3cm
Trace Width=5mils
Trace Resistance>80mohm

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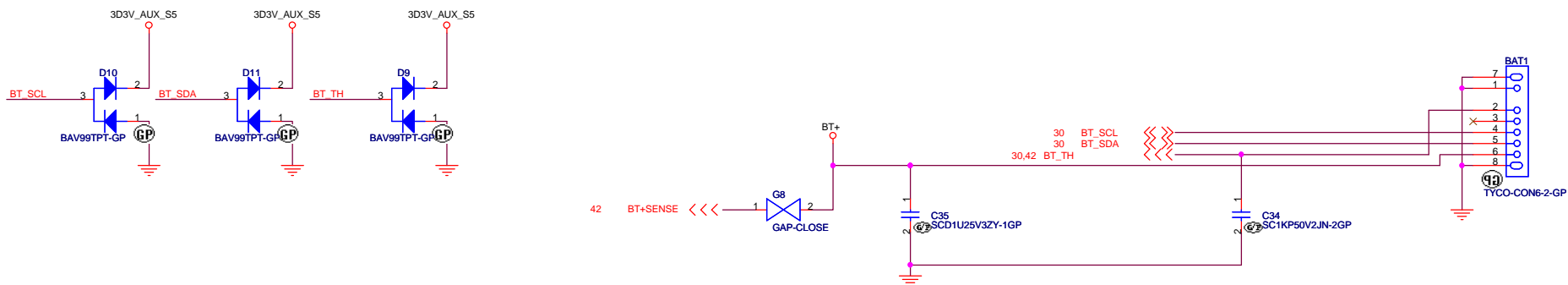
Title			1D5V/2D5V/3D3V/5V_AUX
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Adaptor in to generate DCBATOUT



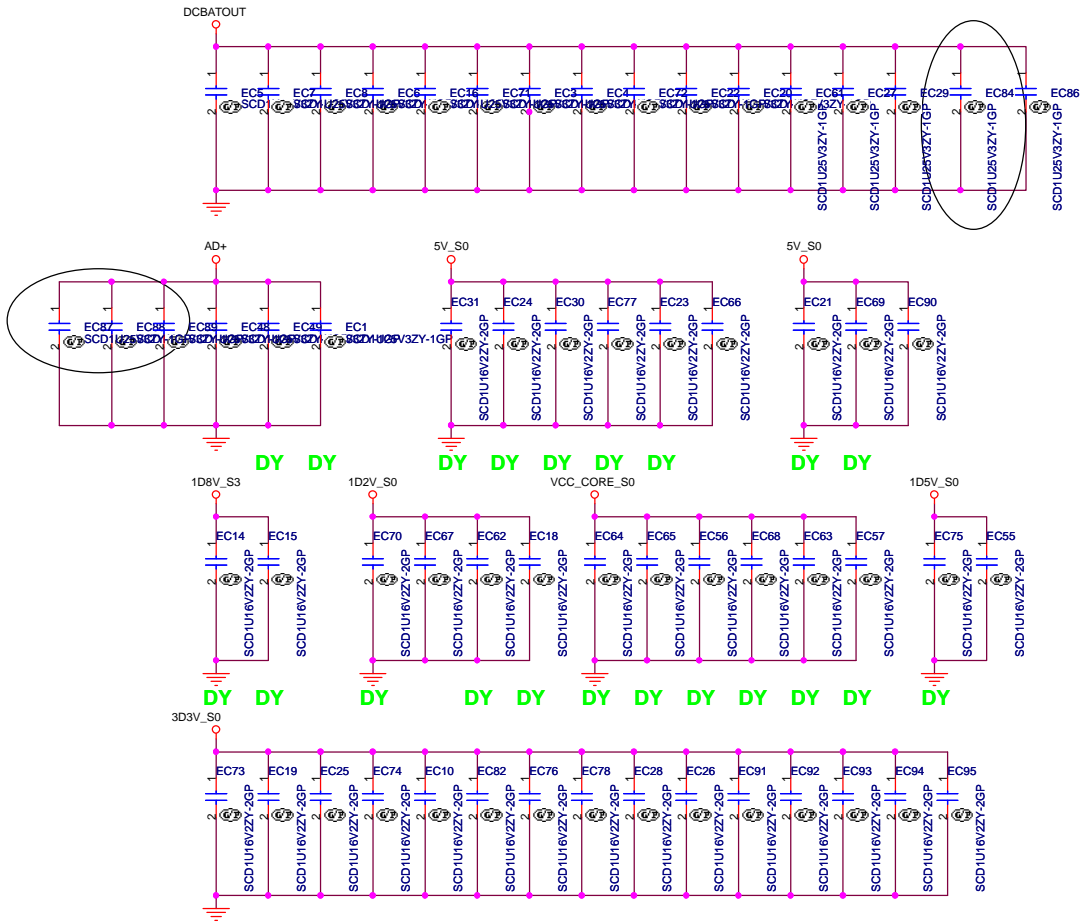
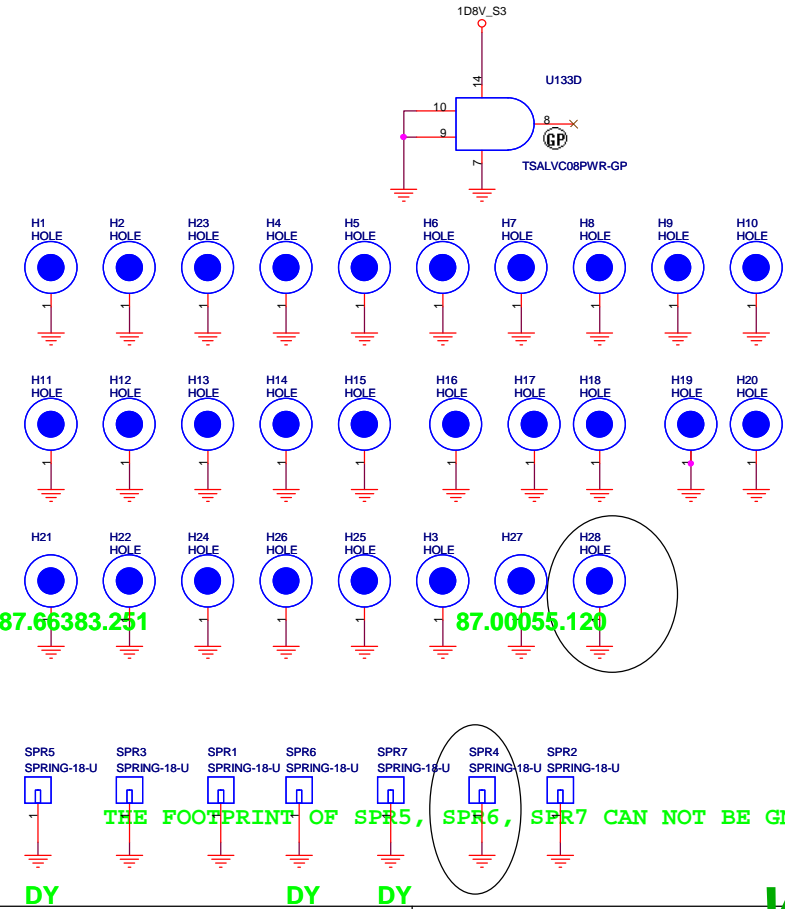
BATTERY CONNECTOR



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	FF	DF
CAMERA	○	×
LAN	10/100	10/100
1394/5 IN 1	○	×
EXTRA USB	○	×
MIC	○	×
CR LED	○	×



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Title		
MISC		
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A3		SA
Date:	Saturday, March 04, 2006	Sheet 44 of 44